CMOS Logic

ECE 320 Electronics I

Jake Glower - Lecture #24

Please visit Bison Academy for corresponding lecture notes, homework sets, and solutions

CMOS Logic

TTL logic is used widely, but has a few limitations:

- The input impedance is not infinity. This limits the fanout.
- The corresponding power consumption is somewhat high (5mW computed previously).
- The maximum clock frequency is limited to about 1MHz (DTL) or 10MHz (TTL)

CMOS logic avoids these problems.

For the following circuits, assume

$R_{ds} = 1\Omega$ @ Vgs = 5V

CMOS Inverter

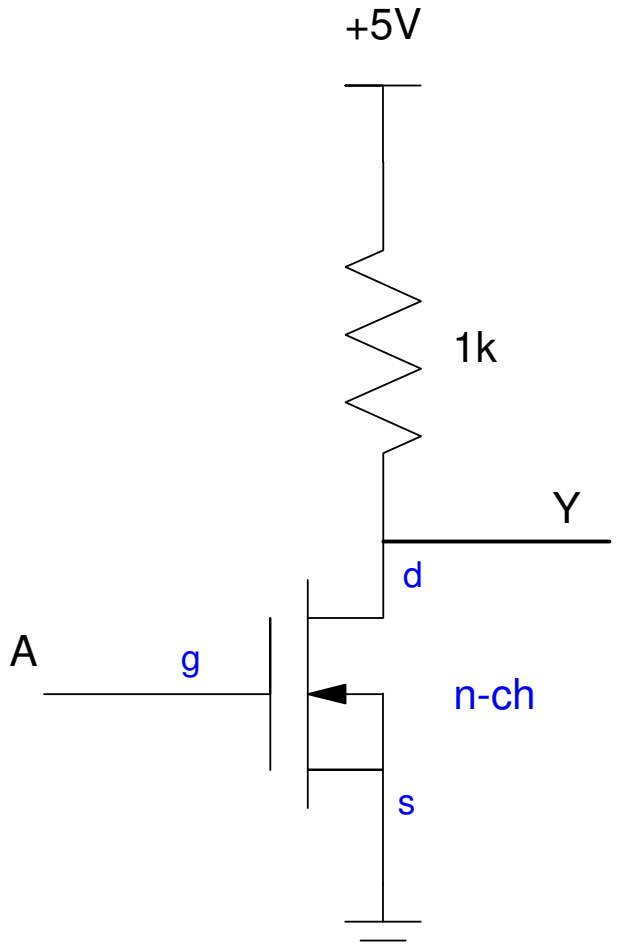
Version 1: n-channel MOSFET.

- Whan $V_A = 0V$, the MOSFET is off. R_{ds} = infinity
- When $V_A = 5V$, the MOSFET is on: R_{ds} = 1 Ohm (approx)

V_A	R_{high}	R_{low}	Y
0V	1,000	infinity	+5V
5V	1,000	1 Ohm	0.005V

Note that this is an inverter:

$$Y = \overline{A}$$



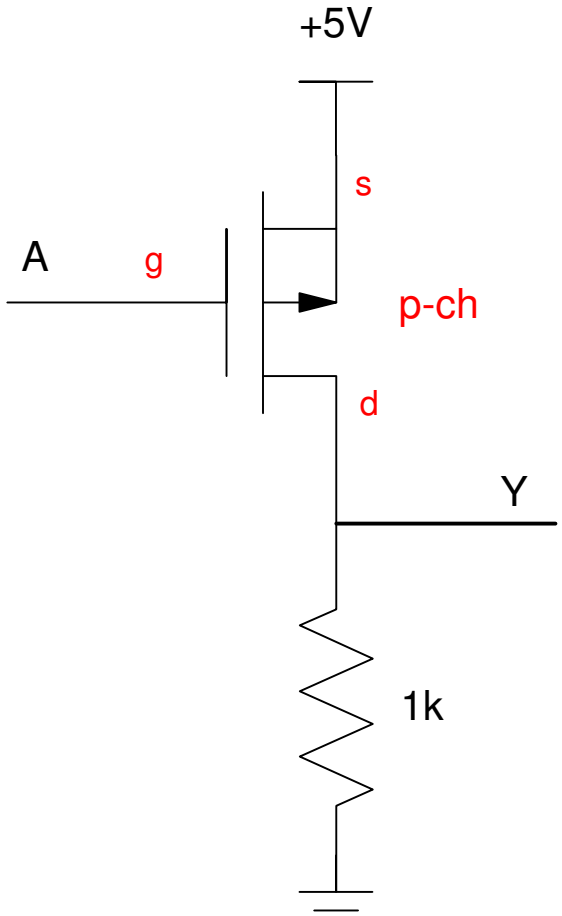
Version 2: p-channel MOSFET

Whan $V_A = 5V$ ($V_{gs} = 0V$)

- The MOSFET is off. R_{ds} = infinity

When $V_A = 0V$ ($V_{gs} = -5V$)

- The MOSFET is on: R_{ds} = 1 Ohm (approx)



This results in the same table:

V_A	R_{high}	R_{low}	Y
0V	1 Ohm	1k	4.995 V
5V	infinity	1k	0.V

Again, note that this is an inverter

$$Y = \overline{A}$$

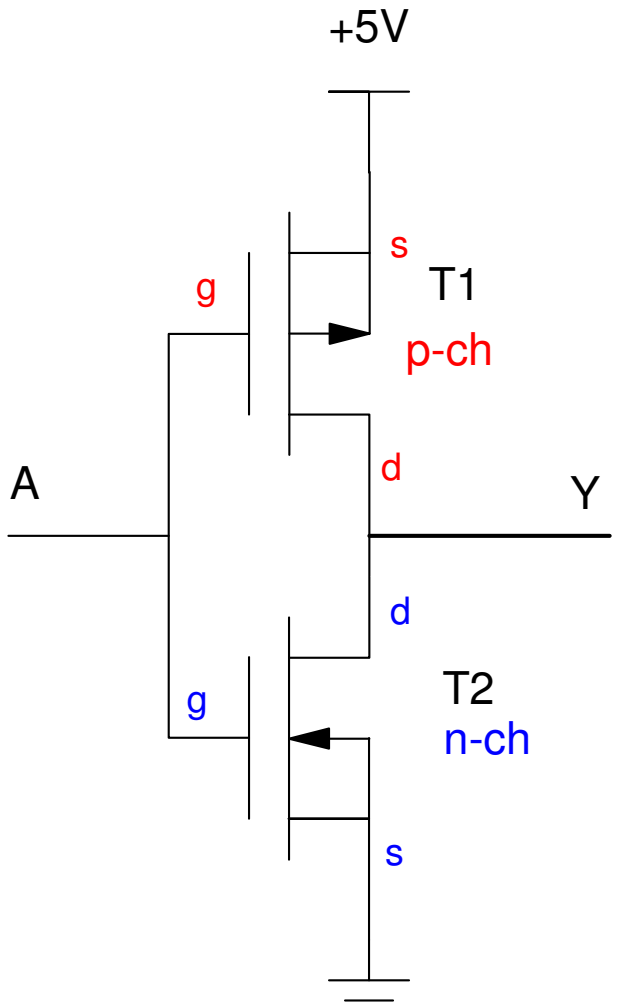
Version 3: Actual CMOS Inverter

- Ids = 0
- One of the MOSFETs are always off

VA	Rhigh (T1)	Rlow (T2)	Y
0V	1 Ohm	infinity	5.00 V
5V	infinity	1 Ohm	0.00 V

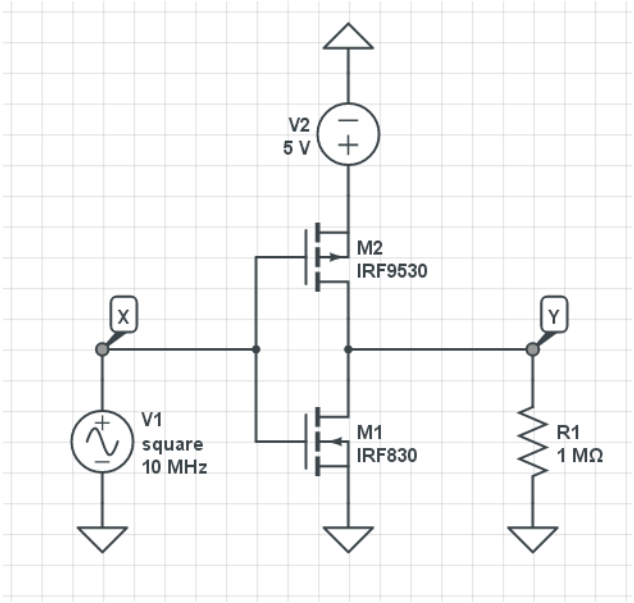
Note: There will be a slight current draw on 0/1 and 1/0 transistions

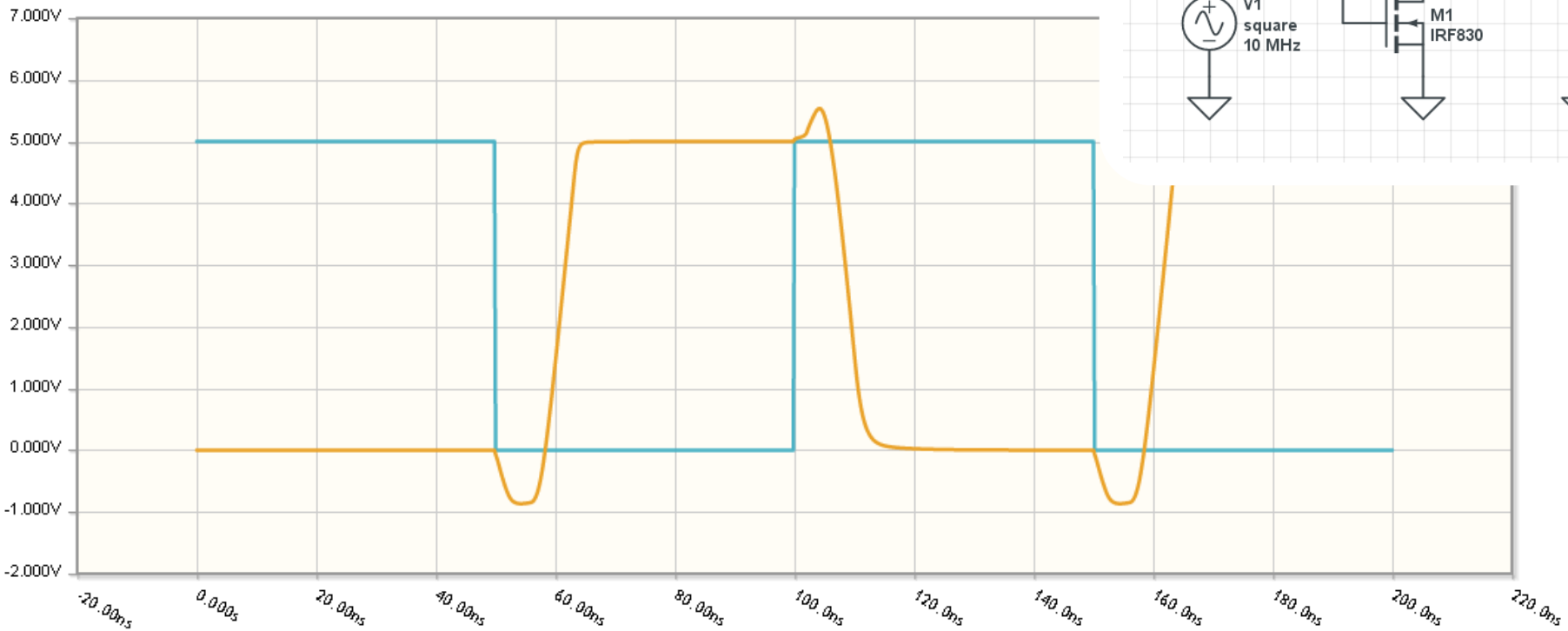
- Both MOSFETs are on momentarily



Max Frequency (CircuitLab)

- Default MOSFET (IRF9530)
- Overkill: 100V & 12A continuous
- T(on) = 12ns
- f(max) = 80MHz



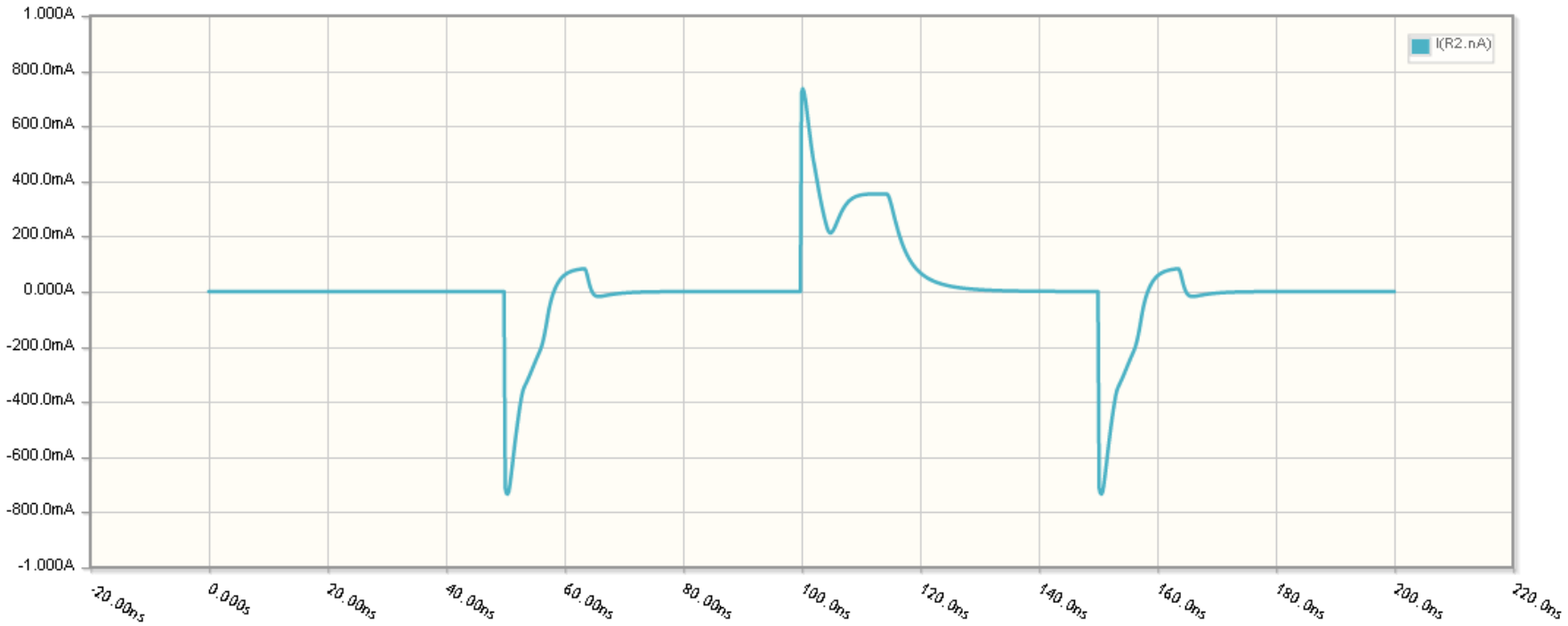


Current Spikes

Like DTL and TTL logic, you get current spikes on 1/0 and 0/1 transitions

- Both MOSFETs momentarily on

Current is proprotional to clock speed with CMOS logic

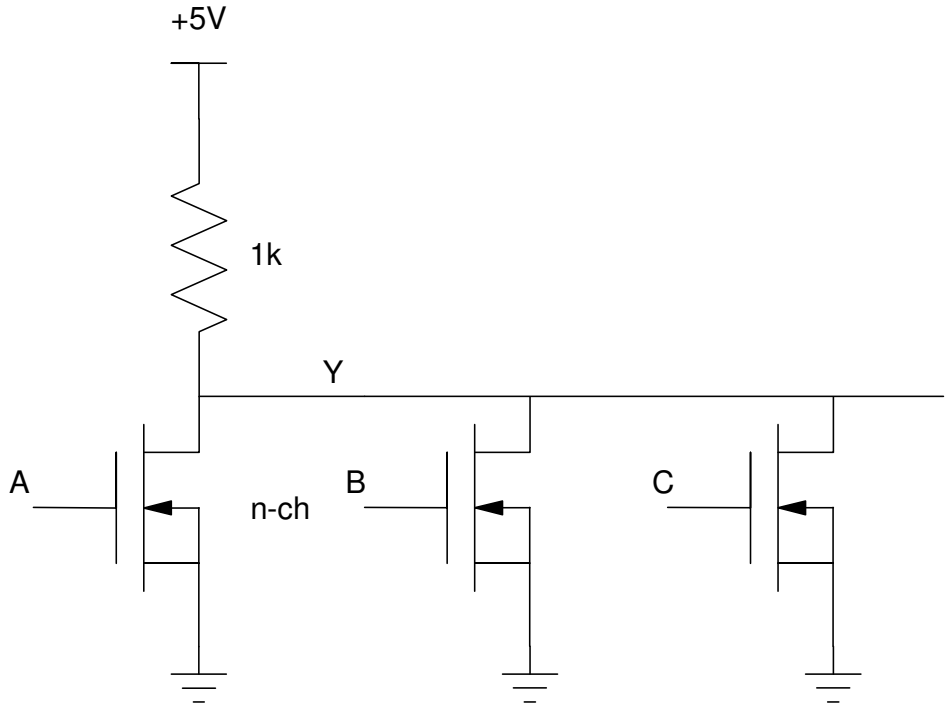


CMOS NOR gate:

- Low side (n-channel)

$$\overline{Y} = A + B + C$$

$$Y = \overline{A + B + C}$$



High Side

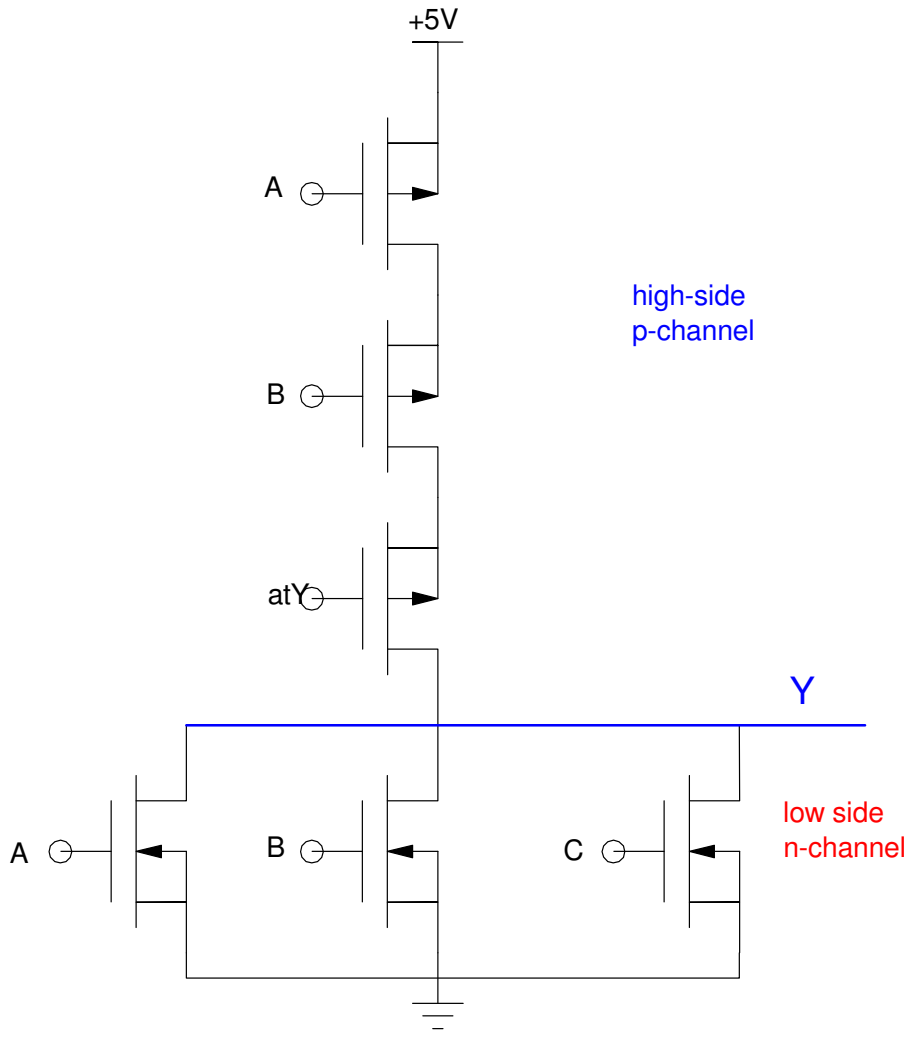
- p-channel MOSFETs
- Related by DeMorgan's theorem
- Note that 0V is on, 5V is off on the high side

$$Y = \overline{A + B + C}$$

$$Y = \overline{A}\,\overline{B}\,\overline{C}$$

Net Result:

- No current draw when on or off
- Spikes on 0/1 and 1/0 transistions



CMOS NAND gate:

Low Side:

- n-channel MOSFETs

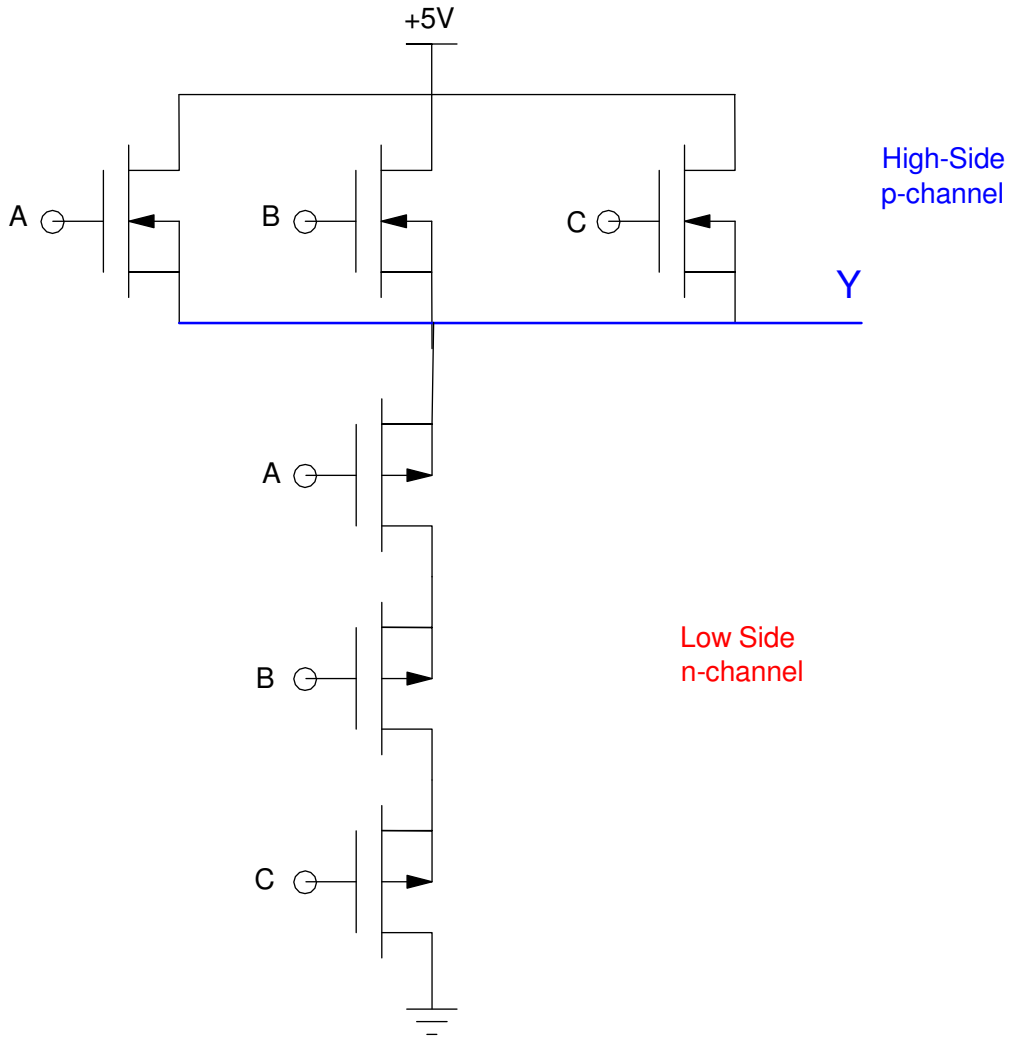
$$\overline{Y} = ABC$$

$$Y = \overline{ABC}$$

High-Side

- p-channel MOSFETs
- Related by DeMorgan's theorem

$$Y = \overline{A} + \overline{B} + \overline{C}$$



CMOS Combinational Logic:

You don't need to use NAND and NOR gates with CMOS logic

You can implement the entire funciton in one gate

- AND = series
- OR = parallel
- high-side and low-side are related by DeMorgan's theorem

CMOS Logic Example:

$$Y = \overline{A}\,\overline{B} + \overline{C}$$

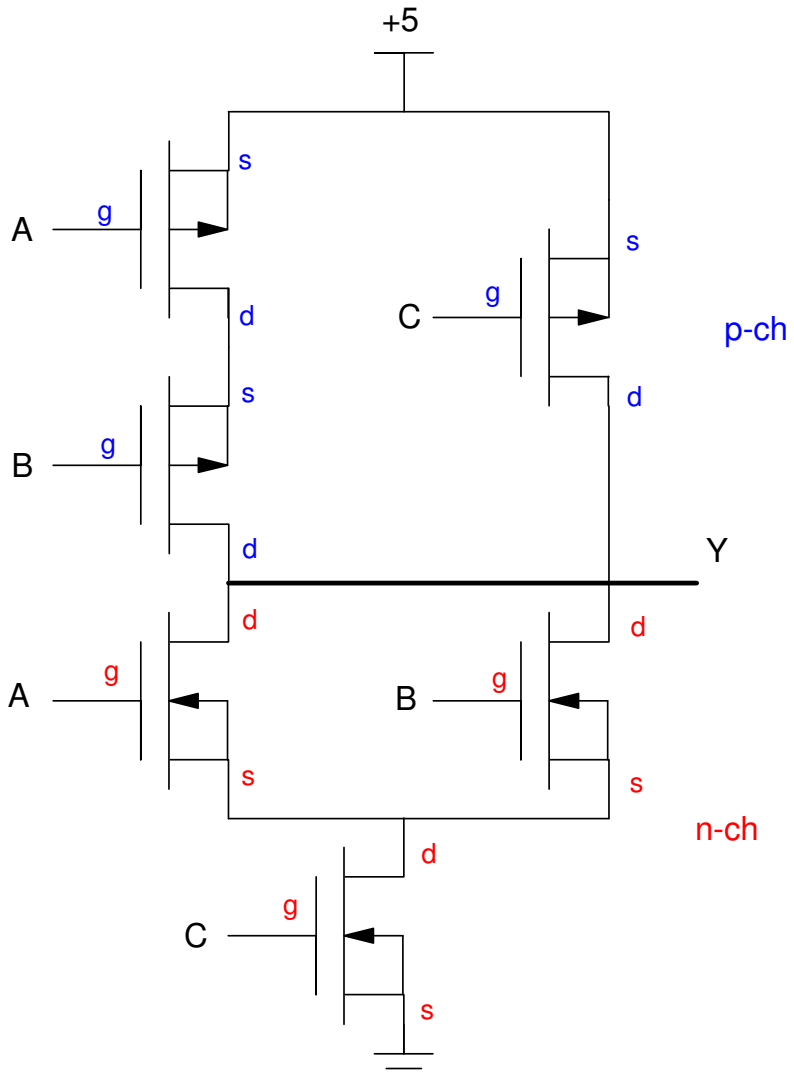
- High-Side:

$$Y = \overline{A}\,\overline{B} + \overline{C}$$

- Low-Side:

$$\overline{Y} = \overline{\overline{A}\,\overline{B} + \overline{C}}$$

$$\overline{Y} = (A + B)C$$



Handout

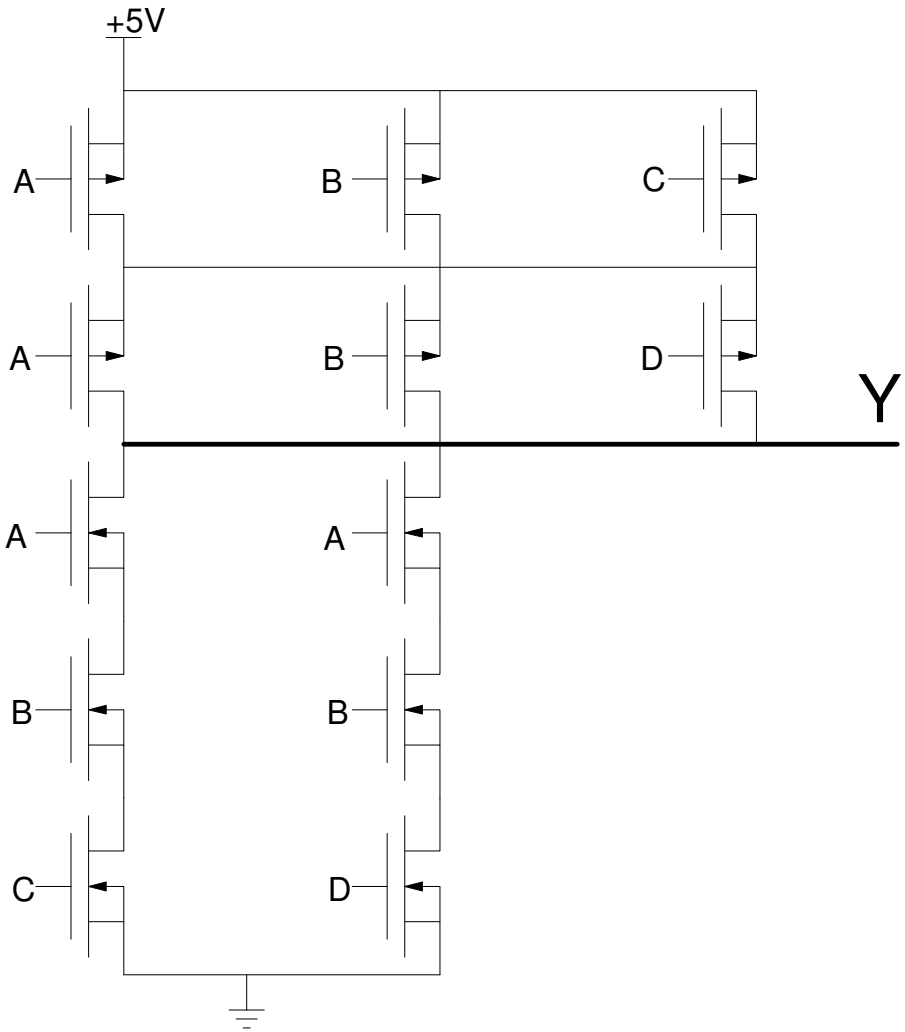
Design a CMOS gate to implement the following logic

Y		CD			
		00	01	11	10
AB	00	1	1	1	1
	01	1	1	1	1
	11	1	0	0	0
	10	1	1	1	1

Solution:

$$\overline{Y} = ABC + ABD$$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	0	0	0
10	1	1	1	1



Summary

CMOS logic

- Draws zero current at logic level 0 or 1
- Can implement an entire funciton in one shot, and
- Is *much* faster than DTL or TTL logic

Current spikes happen at the 0/1 and 1/0 transistions

- Current is proportional to the clock frequency
- Keep digital sections of your circuit away from analog sections