TTL Logic

Transistor Transistor Logic

ECE 320 Electronics I

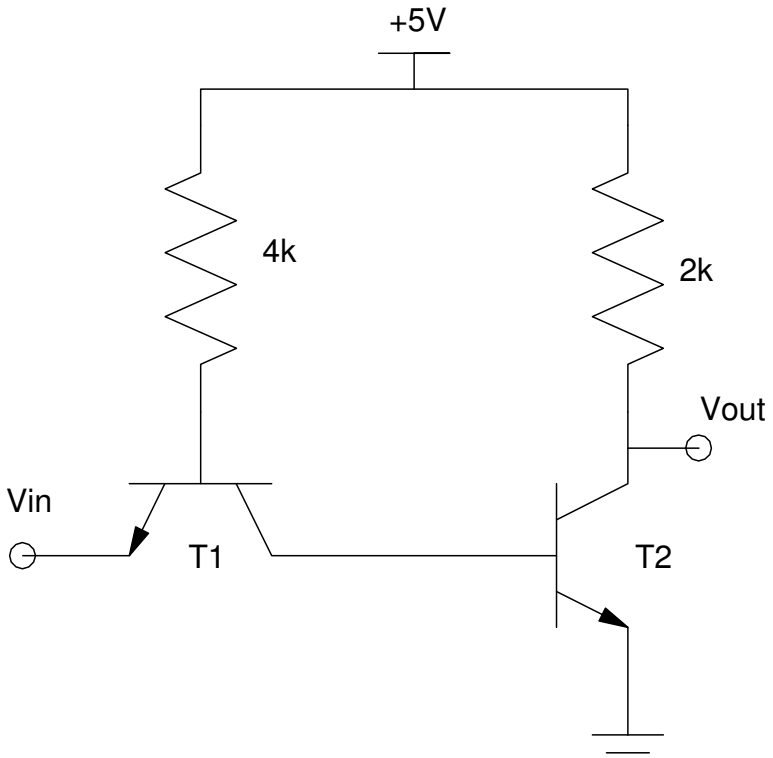
Jake Glower - Lecture #21

Please visit Bison Academy for corresponding
lecture notes, homework sets, and solutions

TTL Logic

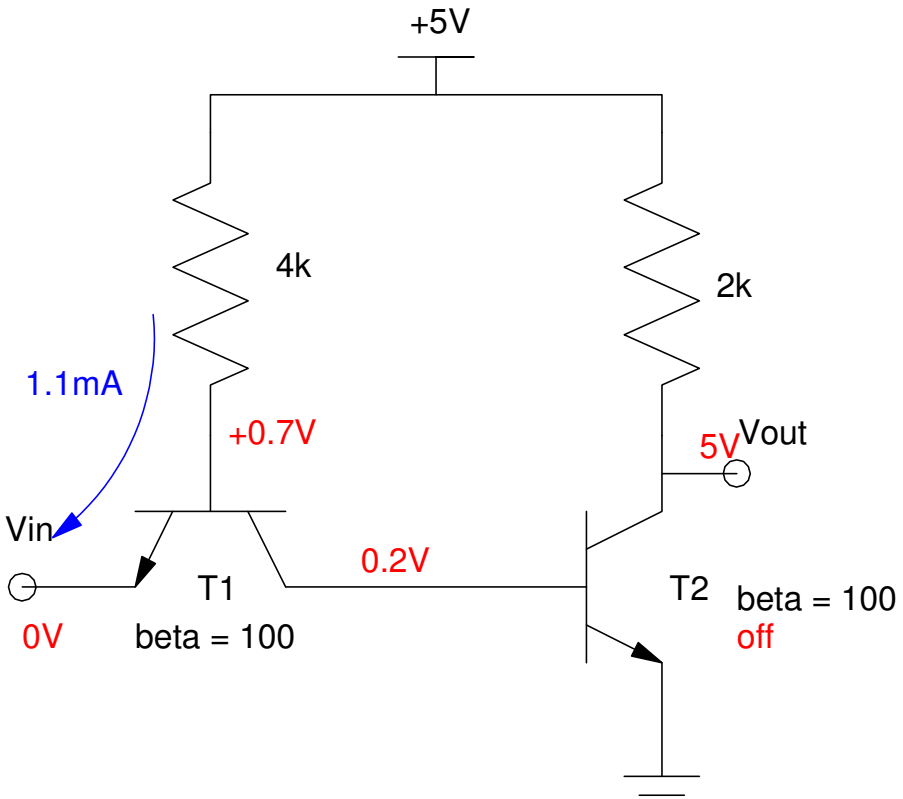
- Diodes are inherently capacitors
- This slows down DTL logic

TTL logic removes the diodes



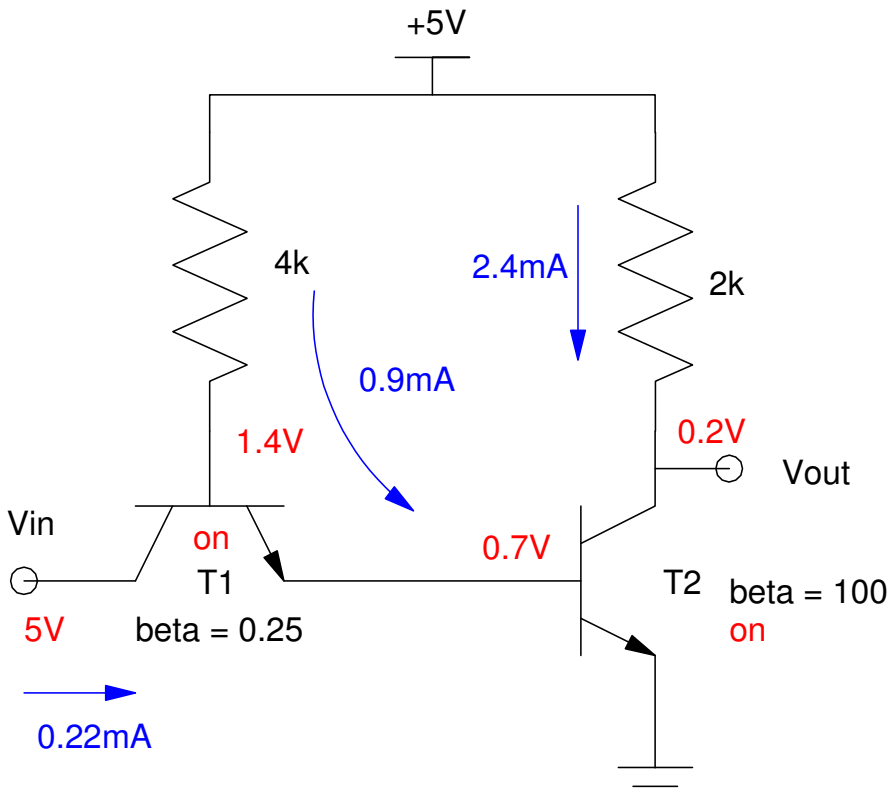
TTL Inverter: Input = Logic 0 (0V)

- T1 saturates
- T2 is off
- Vout = 5V



TTL Inverter: Input = Logic 1 (5V)

- T1 flips (NPN becomes NPN, with lousy gain)
- T1 on (active mode)
- T2 saturates



Power: The power dissipated in this inverter is

Vin = 0V:

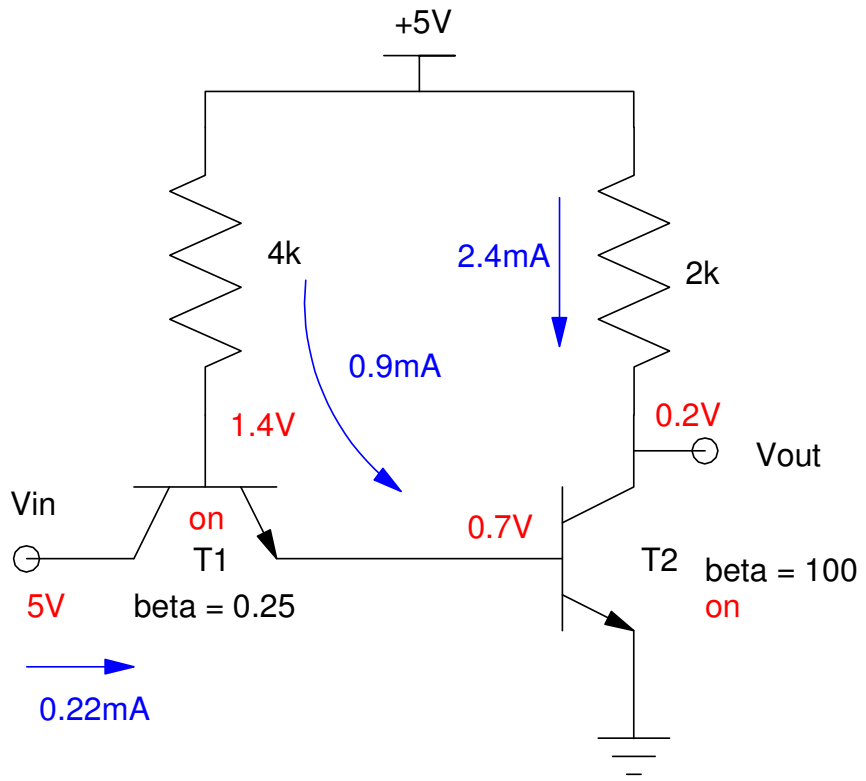
I = 1.1mA

$P = VI = (5V)(1.1mA) = 5.5mW$

Vin = 5V:

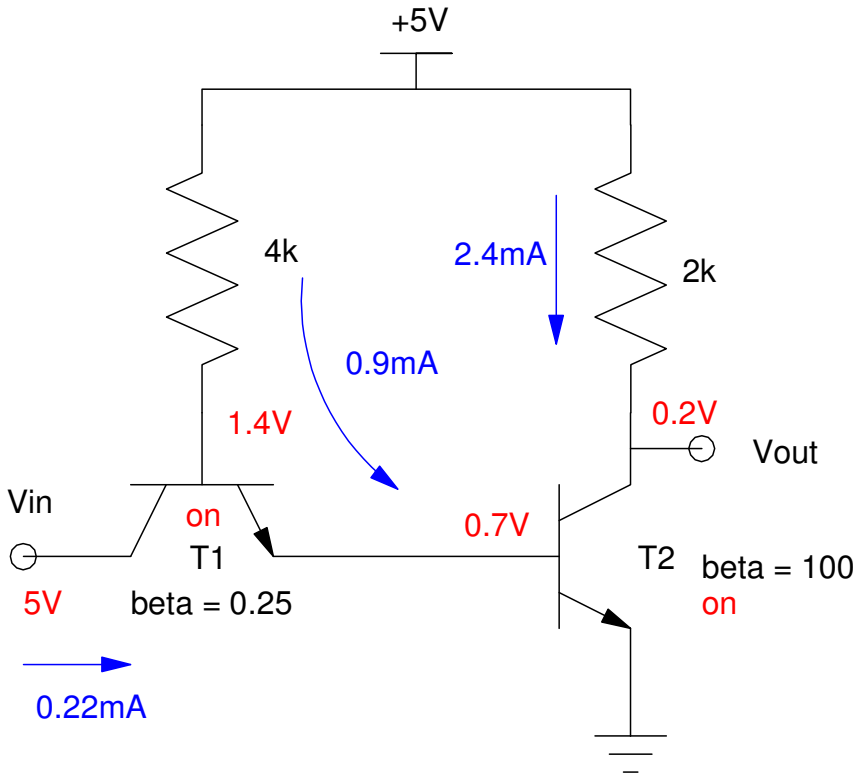
I = 0.9mA + 2.4mA = 3.3mA

$P = VI = (5V)(3.3mA) = 16.5mW$



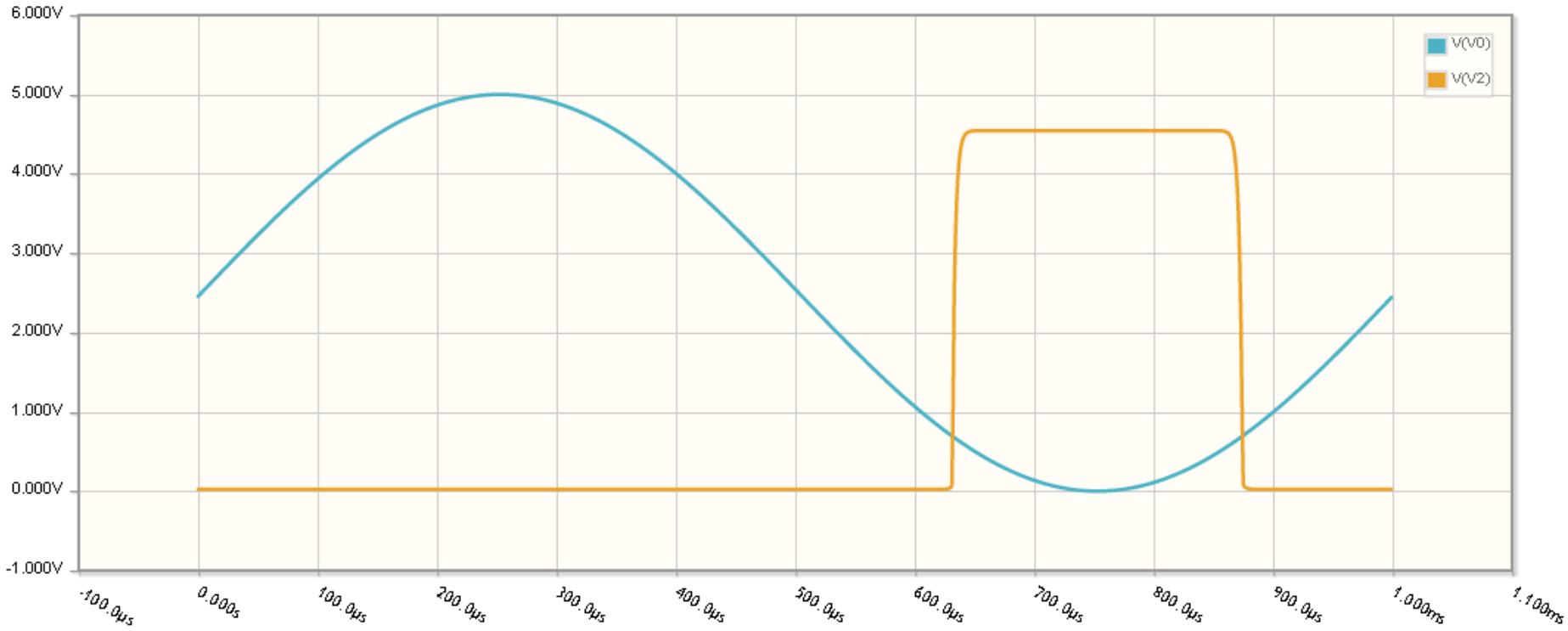
Logic Levels: To turn on T1, Vin > 0.9V: (Vb for T2 is 0.7V. Vce for T1 is about 0.2V. Vin needs to be at least 0.7V + 0.2V).

- Logic Level 0 is a voltage less than 0.9V.
- Logic level 1 is a voltage slightly higher than this.



In CircuitLab, you can test this by sweeping the input voltage and noting when the output is logic level 1 or 0.

- Vin > 700mV Transistor is saturated (Logic level 1 is more than 700mV)
- Vin < 522mV Transistor is off (Logic level 0 is less than 522mV)

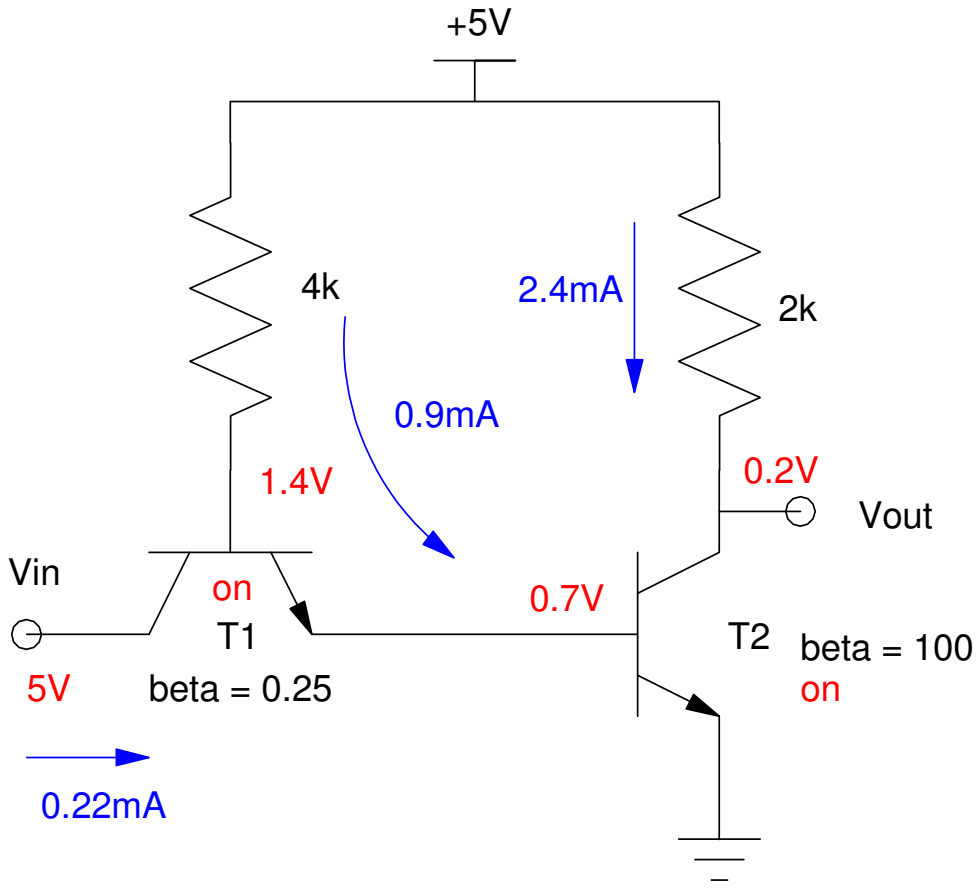


Fanout:

Each load

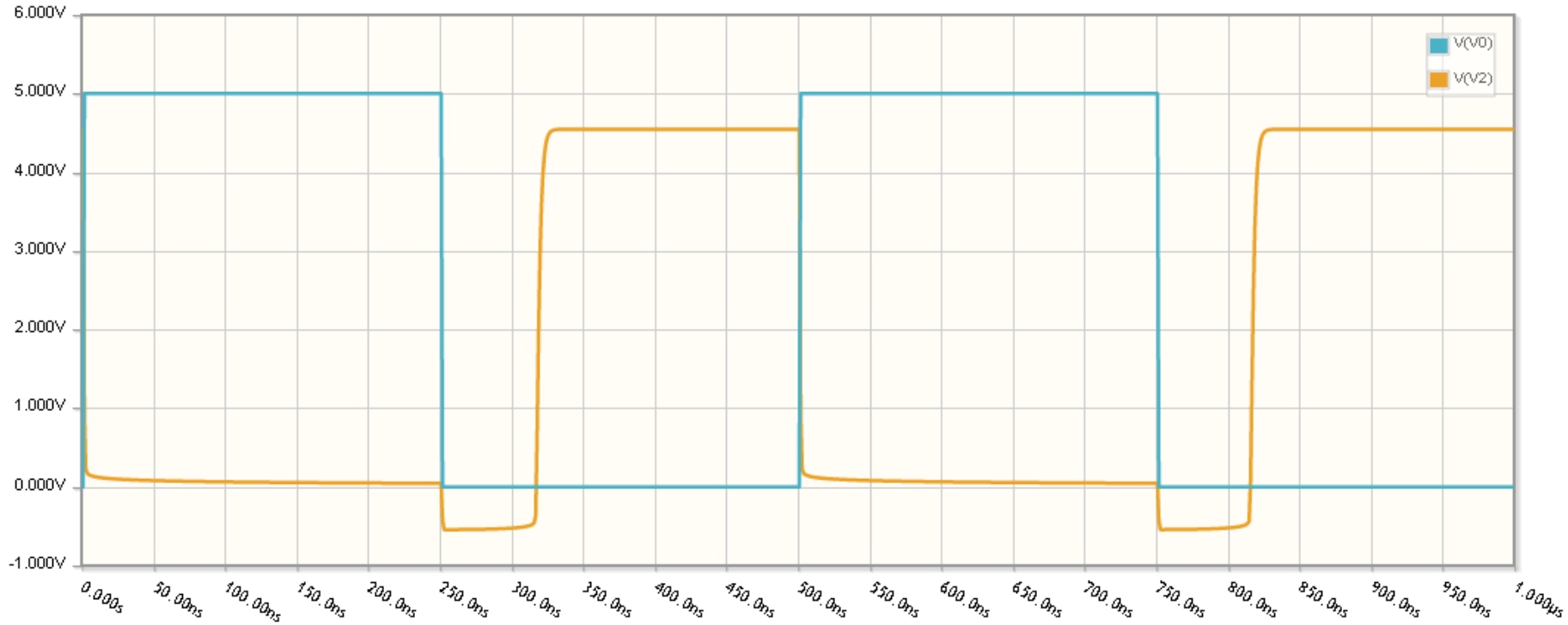
- Draws 0.22mA
- Drops Vout by 0.44V (2k resistor)
- For a 2V drop in Vout, you can have 4 gates

$$N = \frac{2V}{0.44V/gate} = 4.54 \text{ gates}$$



Max Clock Frequency

It takes about 80ns for the output to go from logic level 0 to level 1. This limits the maximum clock frequency to about 10MHz.



CircuitLab simulation of a TTL inverter with 2MHz input.

7400 Series of TTL Inverters

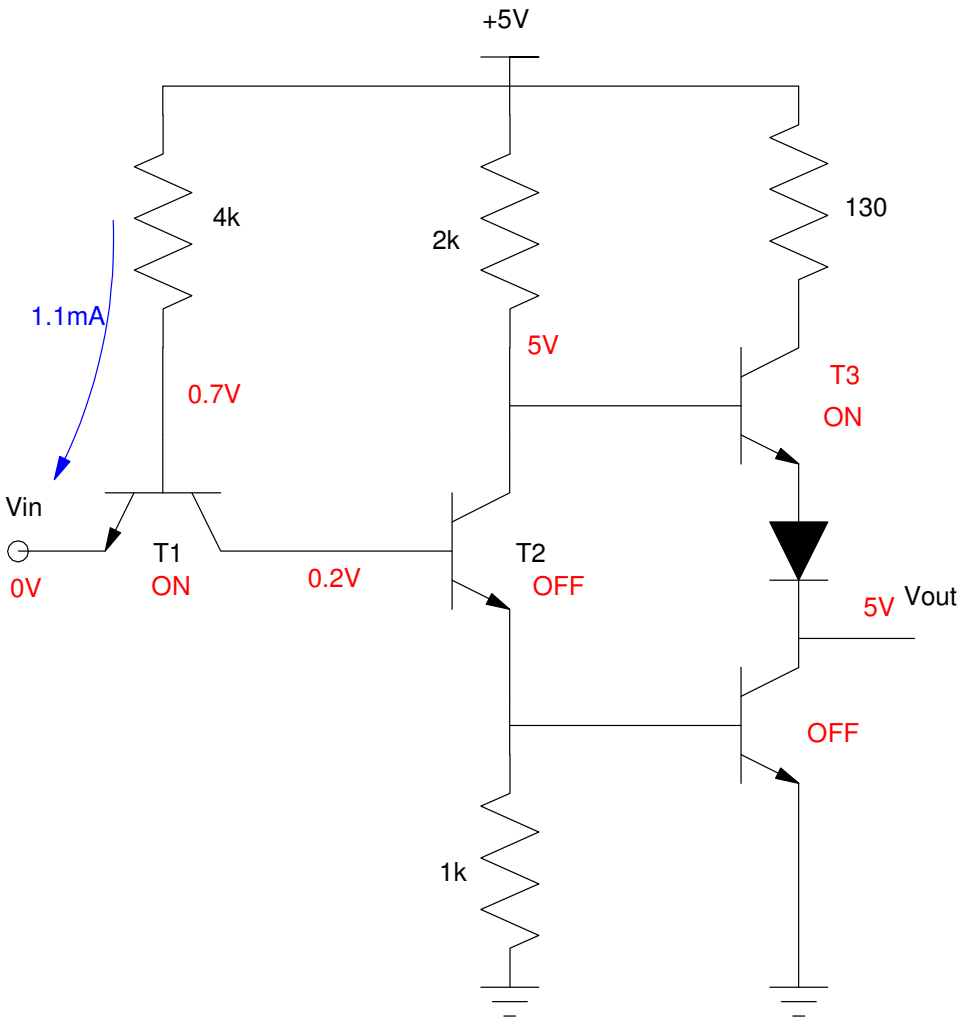
The previous TTL inverter is the heart of the 7400 series inverters.

Assume Vin = 0V

- T1 is on
- T2 is off
- T3 is on
- Vout = 5V

Logic Level 0:

- Vin < 1.6V



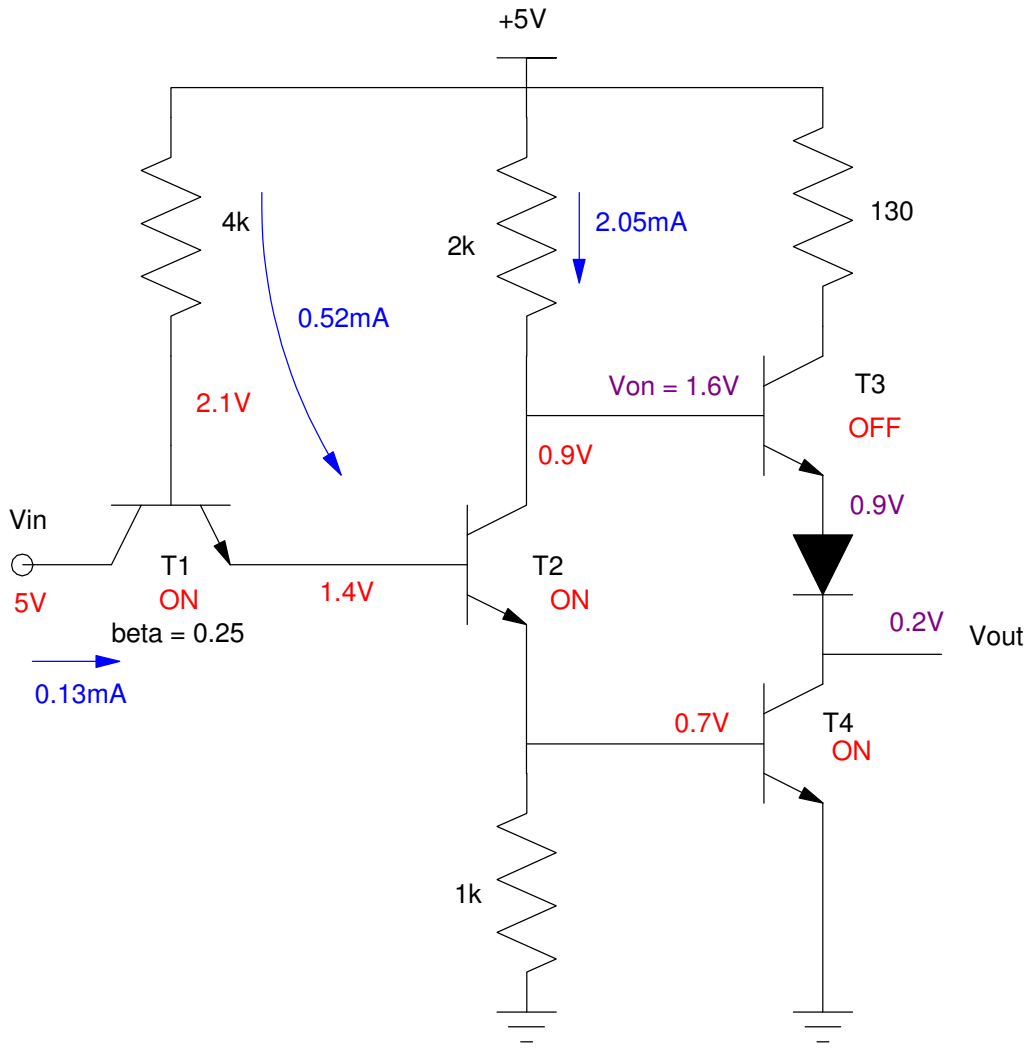
Assume Vin = 5V

- T1 is active
- T2 is saturated
- T4 is saturated

Vout = 0.2V

Logic Level 1:

- Vin > 1.6V



Fanout:

Logic Level 1: Vout > 1.6V

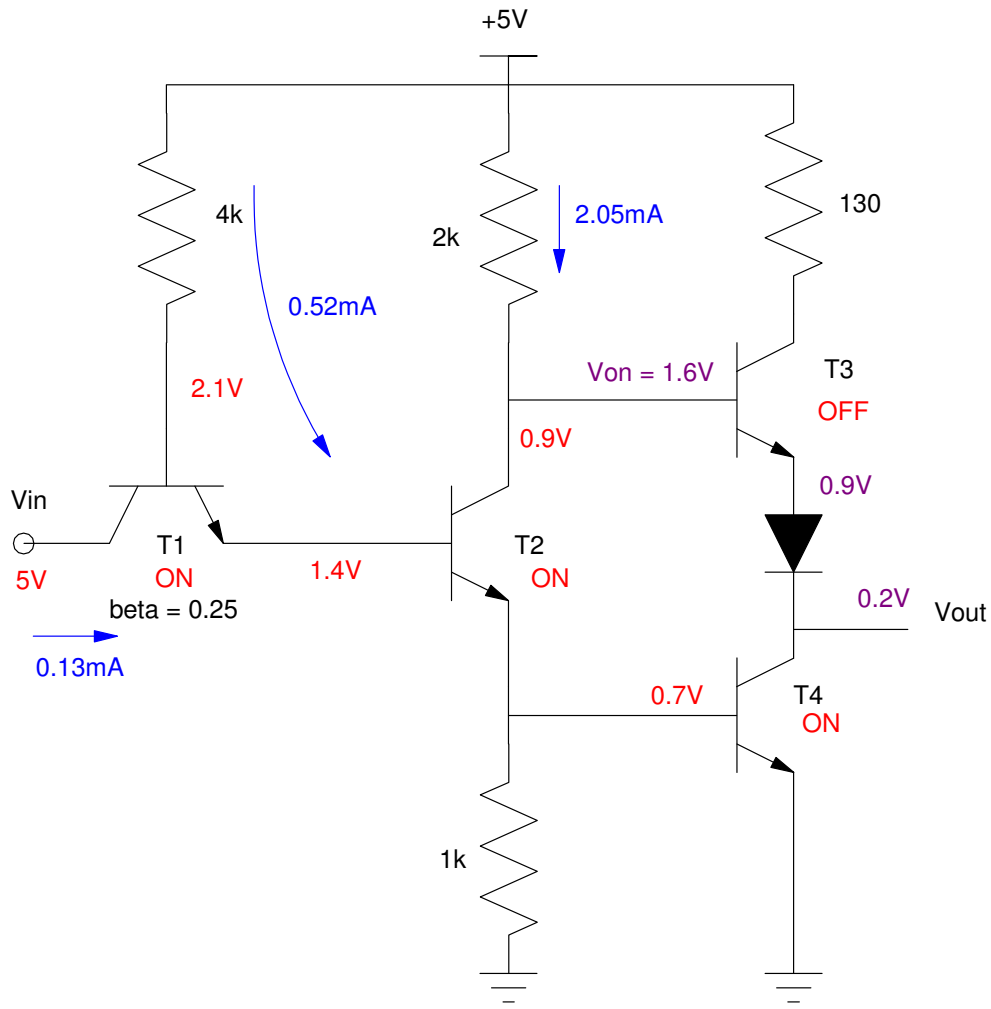
$$V_{out} = 5V - 130\Omega \cdot I - 0.7V > 1.6V$$

Each load draws 0.13mA, so

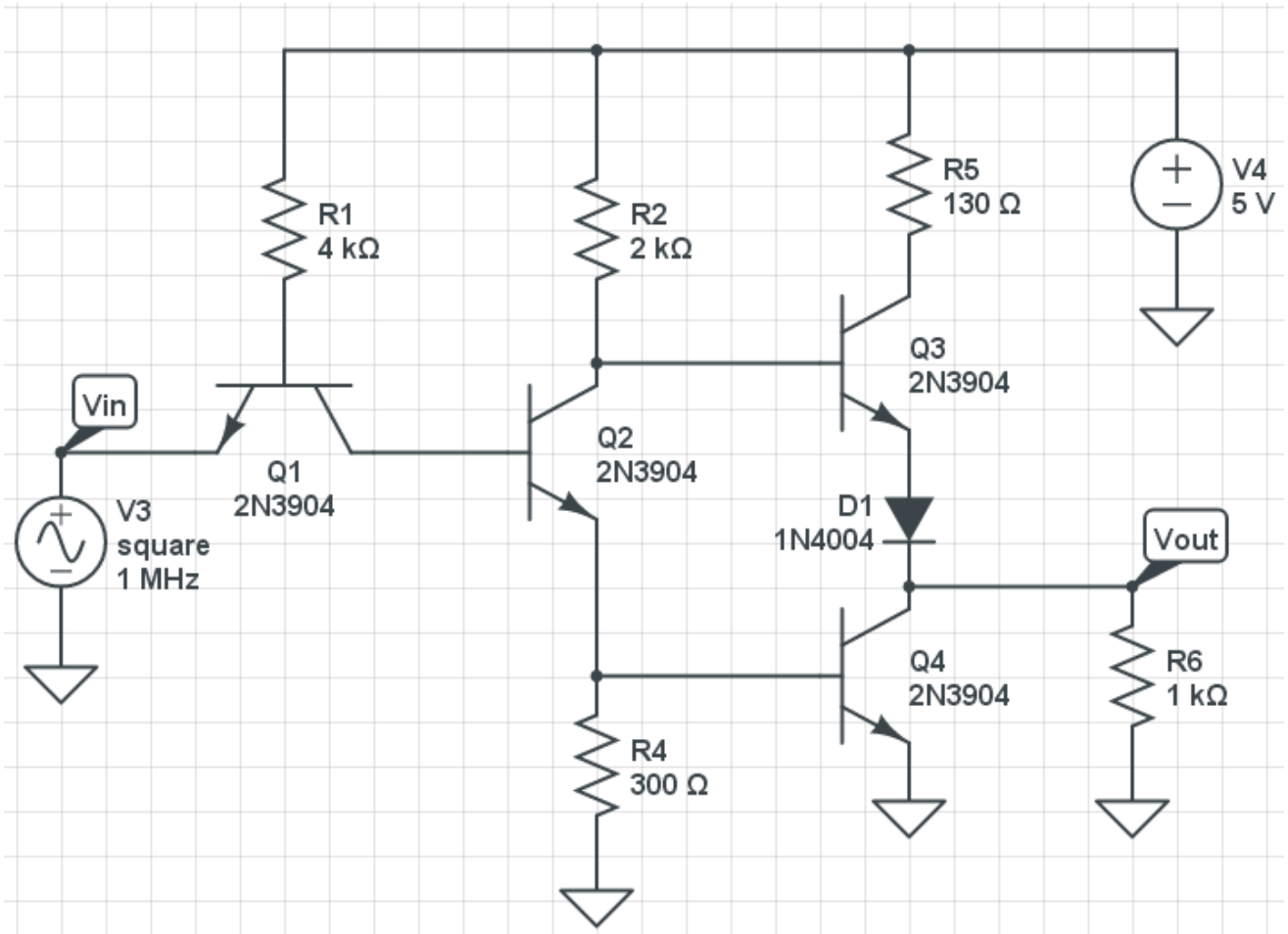
$$5V - 130\Omega \cdot (N \cdot 0.13mA) - 0.7V > 1.6V$$

$$N \leq 159$$

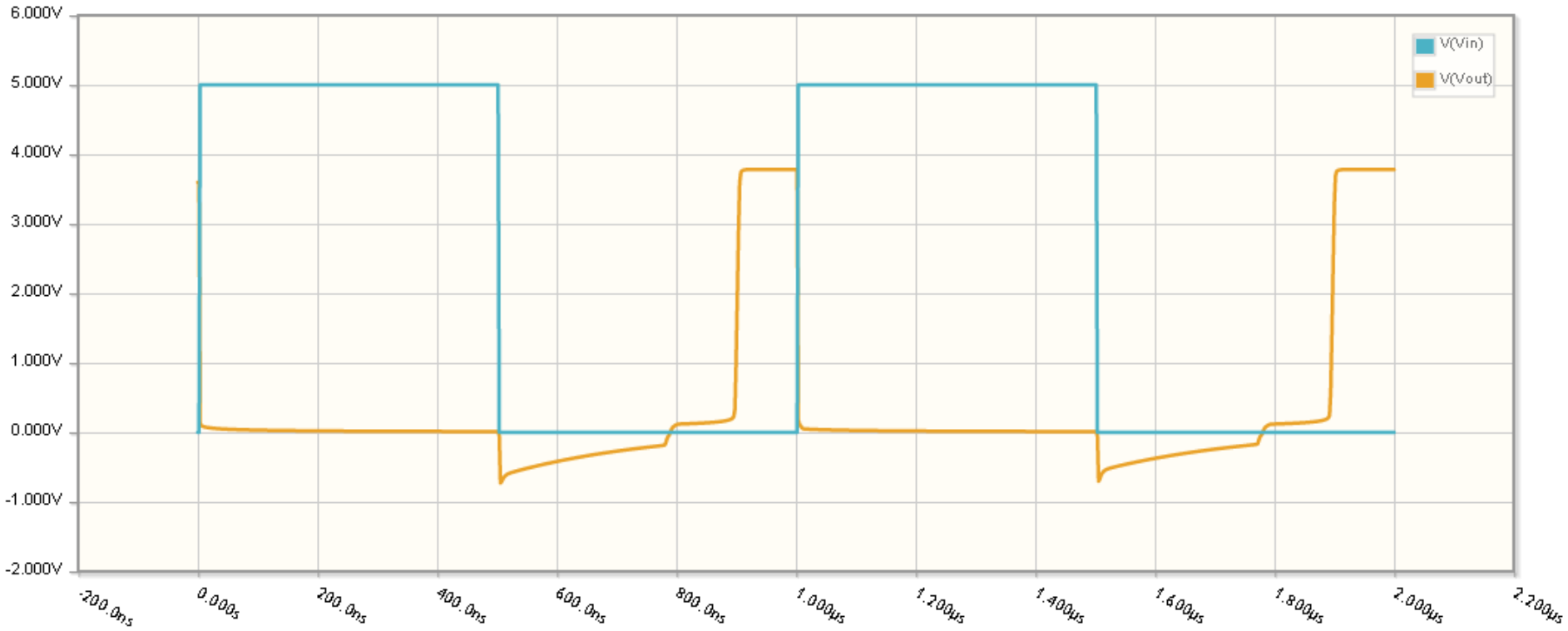
Fanout = 159



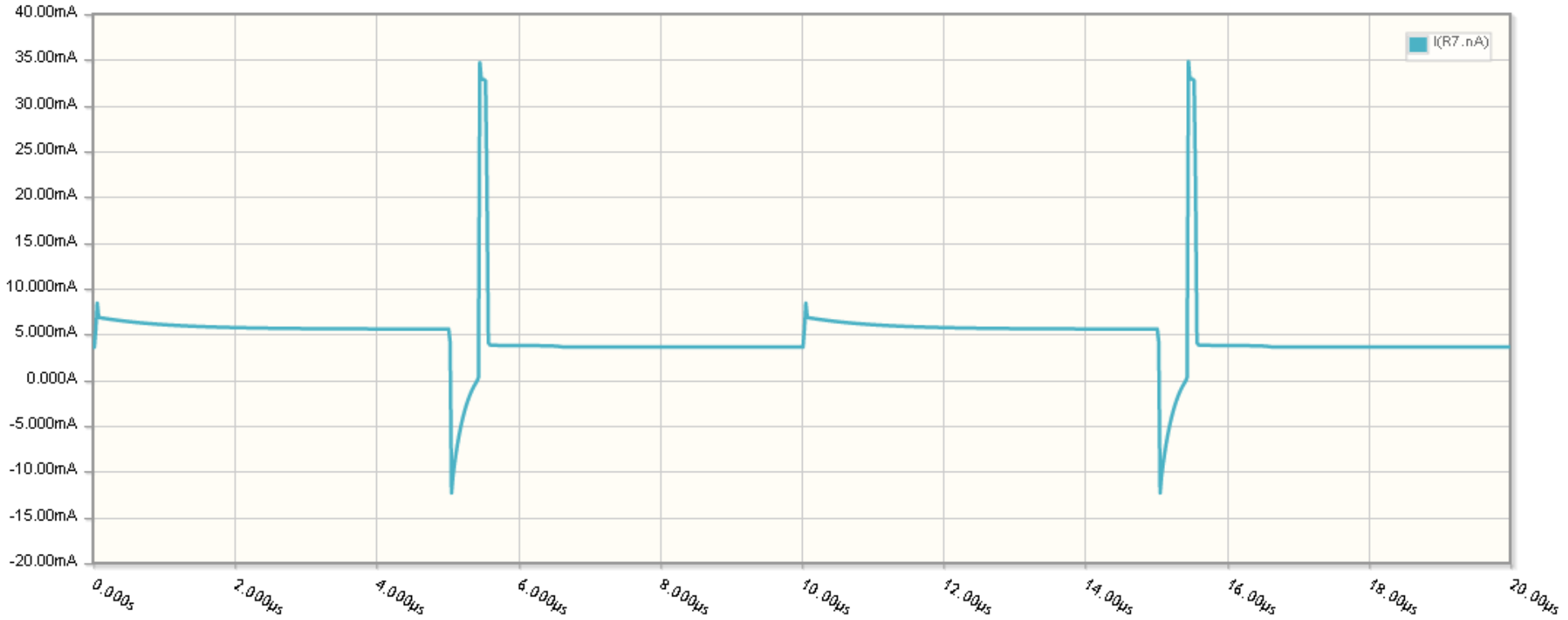
CircuitLab Simulation



7400 TTL inverter for CircuitLab



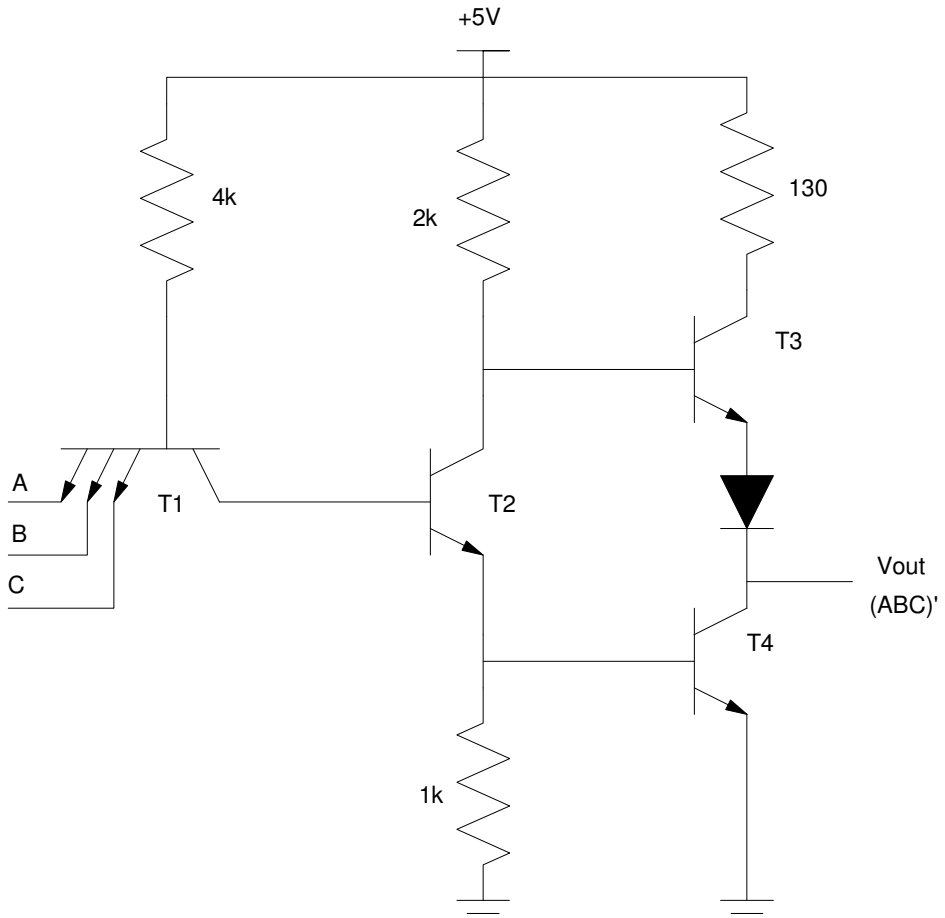
It takes about 400ns to go from logic level 0 to level 1, limiting the clock speed to 2MHz



Current Consumption for TTL Logic. Spikes appear on the current line whenever you have a 1 / 0 transition

TTL NAND gate:

- Add more base pads to T1



Open Collector Outputs:

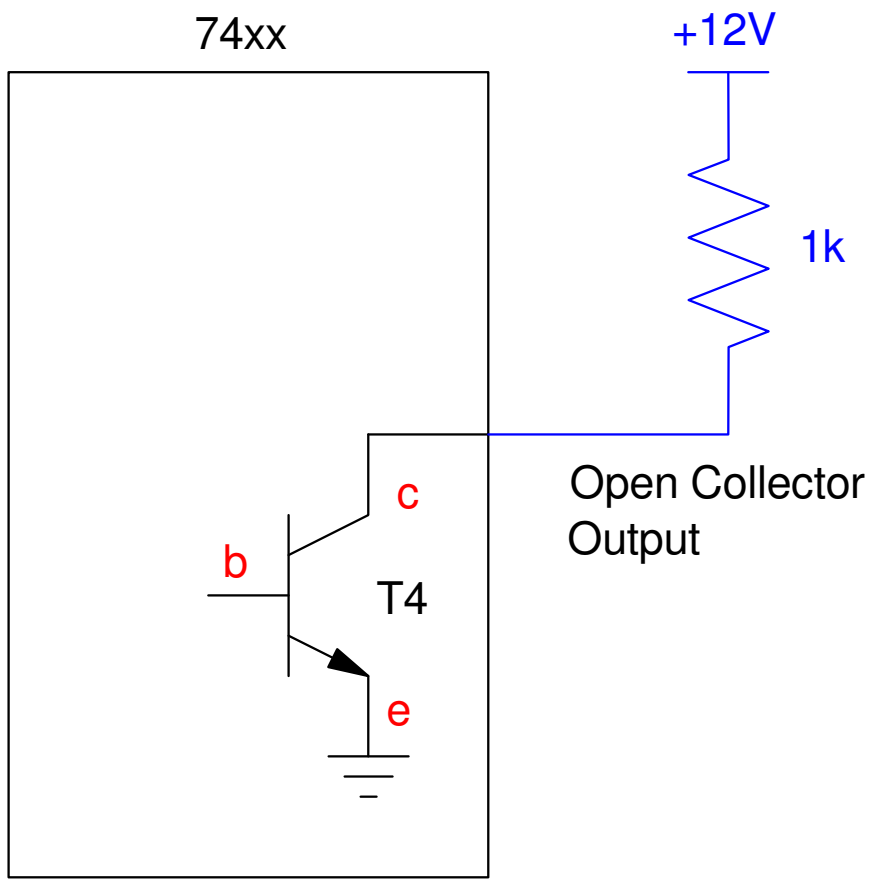
Output is

- Floating (logic 1)
- Ground (logic 0)

Needs a pull-up resistor to see a voltage

Advantages:

- Allows any output voltage (12V)
- Can drive LEDs diretly
- Allows for wire-OR logic



Wirer-OR Logic

Used for CAN bus

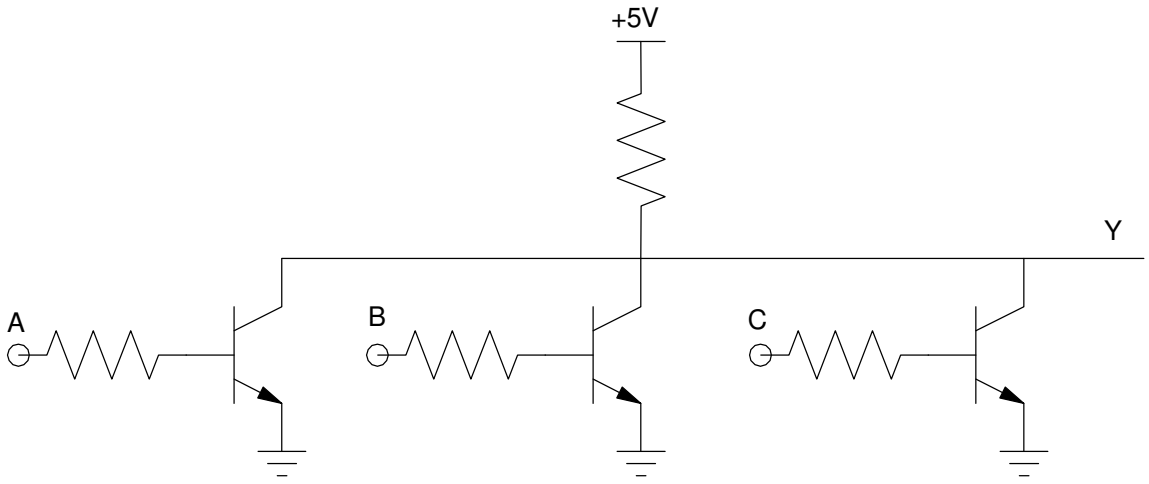
- Zero-priority encoding
- If any driver outputs 0V (transistor saturated), output is 0V

Example:

```
A = 1 1 0 0 1 0 1 1 0
B = 1 1 0 1 1 1 0 1 1
C = 1 0 1 1 0 1 1 1 0
```

C goes first

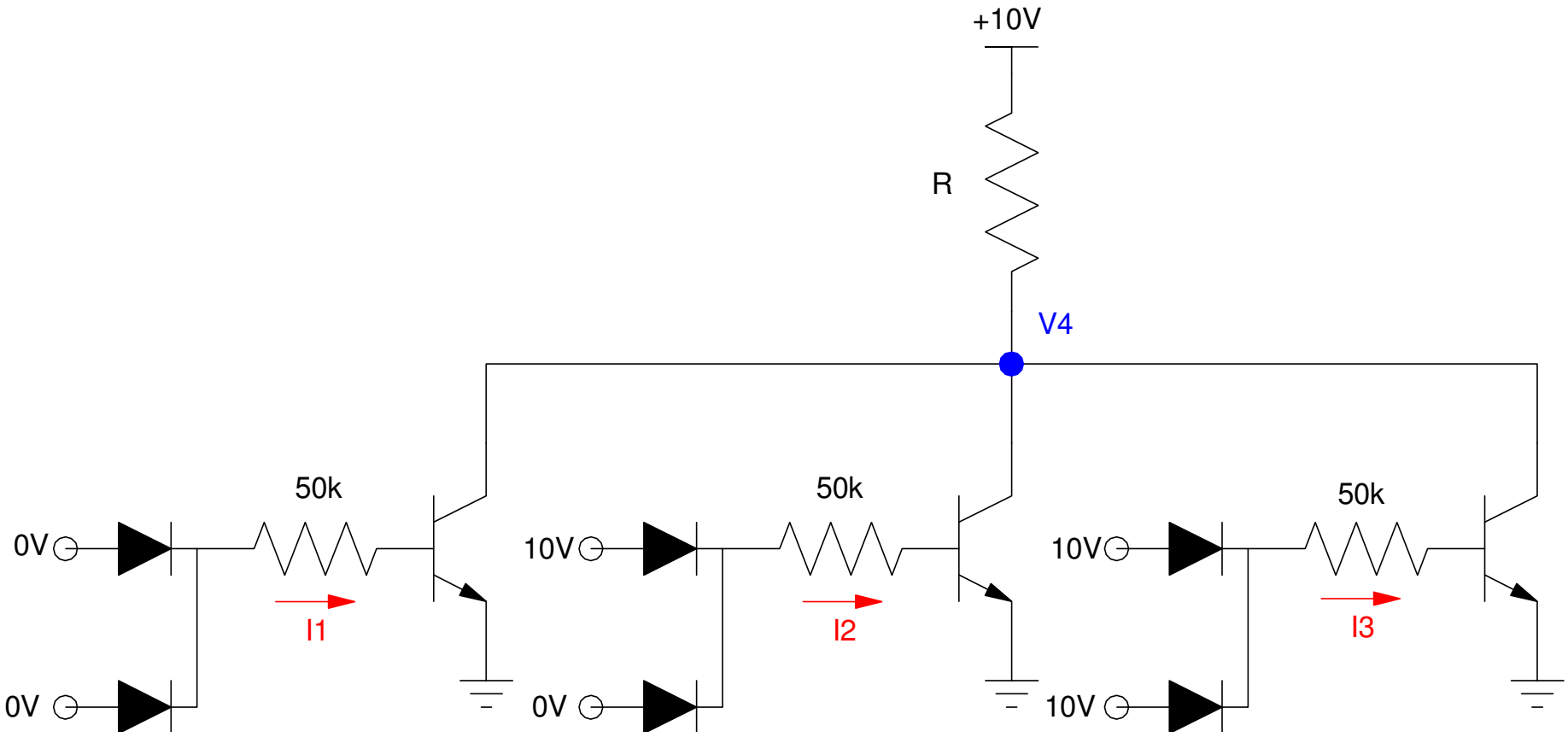
- Then A
- Then B



Wired-Or Example:

Determine the voltages and currents

- Assume 3904 transistors & R = 1k



Summary

TTL Logic is faster than DTL

- Removing the diode removes a capacitor
- Results in faster switching

Wired-or logic allows

- You to shift logic levels (12V instead of 5V), and
- Multiple inputs without conflicts
  - 0V always wins
  - Zero-priority encoding