DTL Logic

Diode Transistor Logic

ECE 320 Electronics I

Jake Glower - Lecture #20

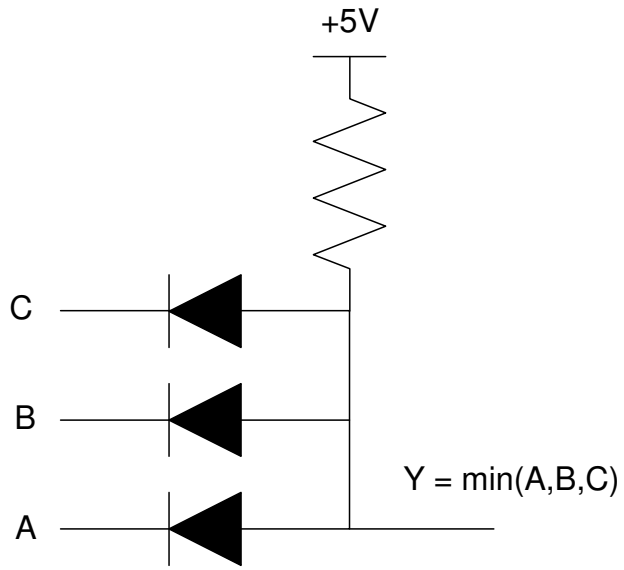
Please visit Bison Academy for corresponding
lecture notes, homework sets, and solutions

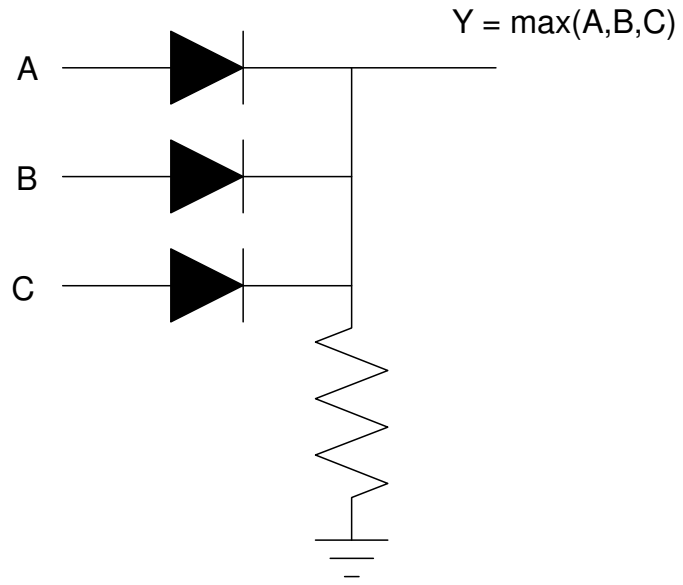
Diode Transistor Logic (DTL)

- min(A,B) = AB
- max(A,B) = A+B

If using fuzzy logic, use diodes in parallel

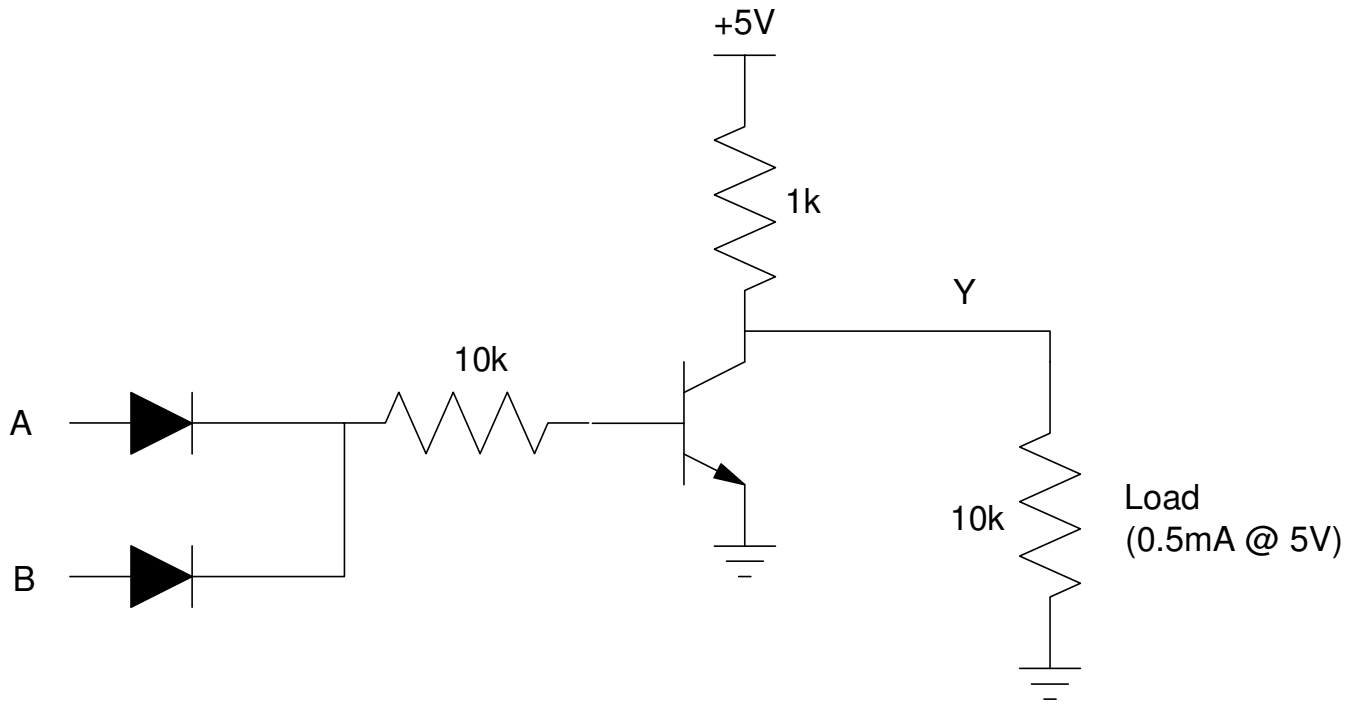
- For Boolean logic, add a transistor to restore logic levels (0V or 5V)





DTL NOR Gate

- max(A, B)
- Cleaned up with a transistor
- Also provides higher fanout and current capability



DTL NOR gate: a max(A,B) function is coupled with a transistor to return the logic levels to 0V / 5V

Analysis: DTL NOR Gate

Case 1: A = 5V, B = 0V.

Ib > 0 (saturates the transistor)

$$I_b = \left(\frac{5V - 1.4V}{10k}\right) = 360\mu A$$

$$\beta I_b = 36mA$$

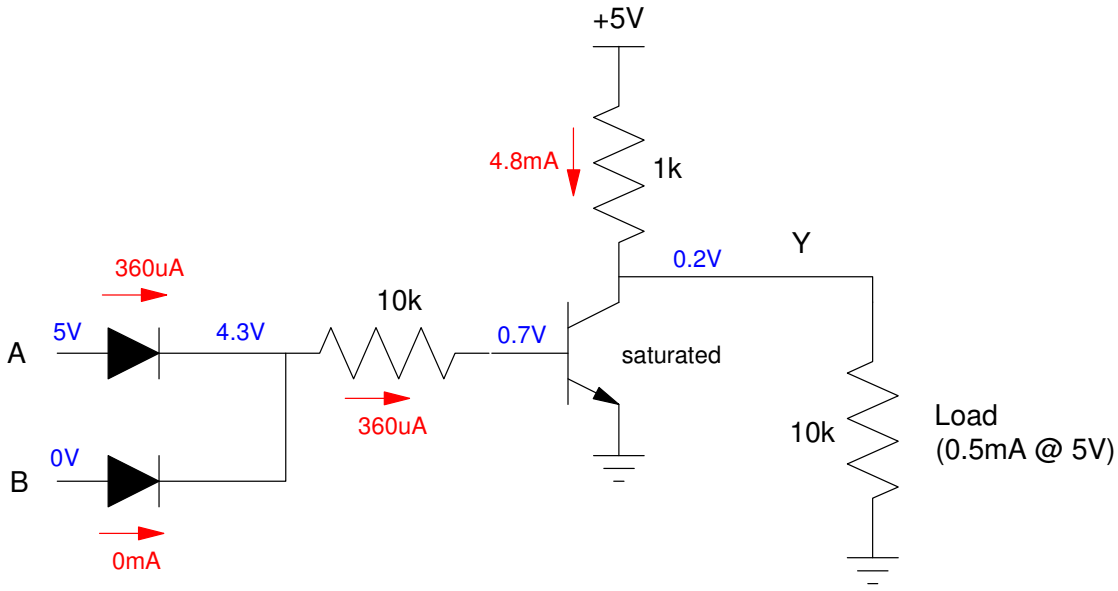
$$\max(I_c) = \left(\frac{5V - 0.2V}{1k}\right) = 4.8mA$$

so the transistor is saturated.

$$\beta I_b > I_c$$

$$36mA > 4.8mA$$

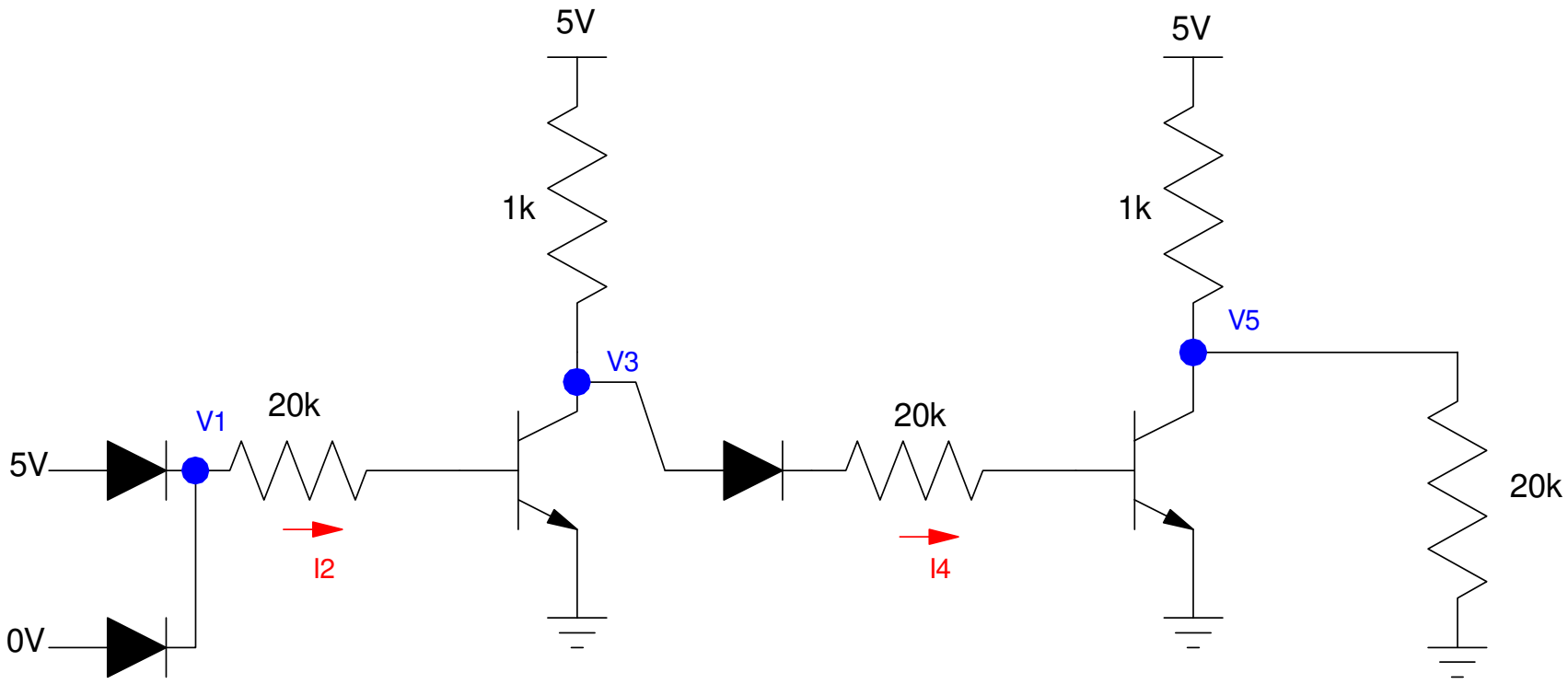
$$Y = 0.2V$$



Handout

Determine the voltages and currents. Assume 3904 transistors

- Vbe = 0.7V
- Vce(sat) = 0.2V



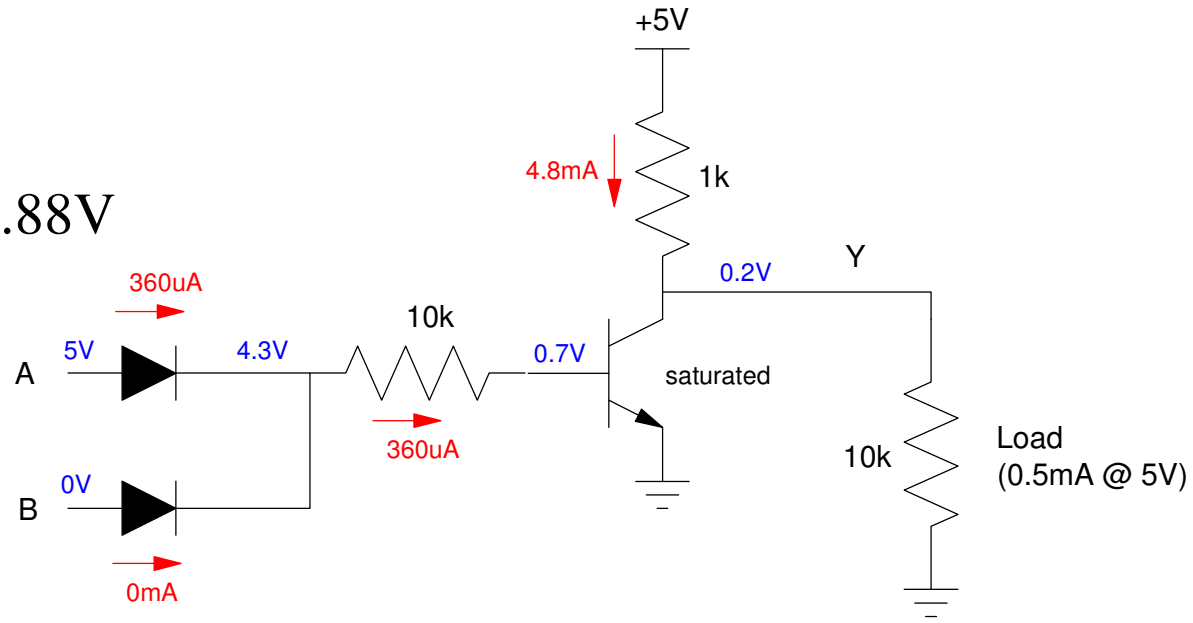
Logic levels:

Transistor remains saturated for Va > 1.88V

$$\left(\frac{V_A - 1.4V}{10k}\right) > 48\mu A$$

$$V_A > 1.88V$$

Logic Level 1 is anything above 1.88V



Case 2: Va = Vb = 0V.

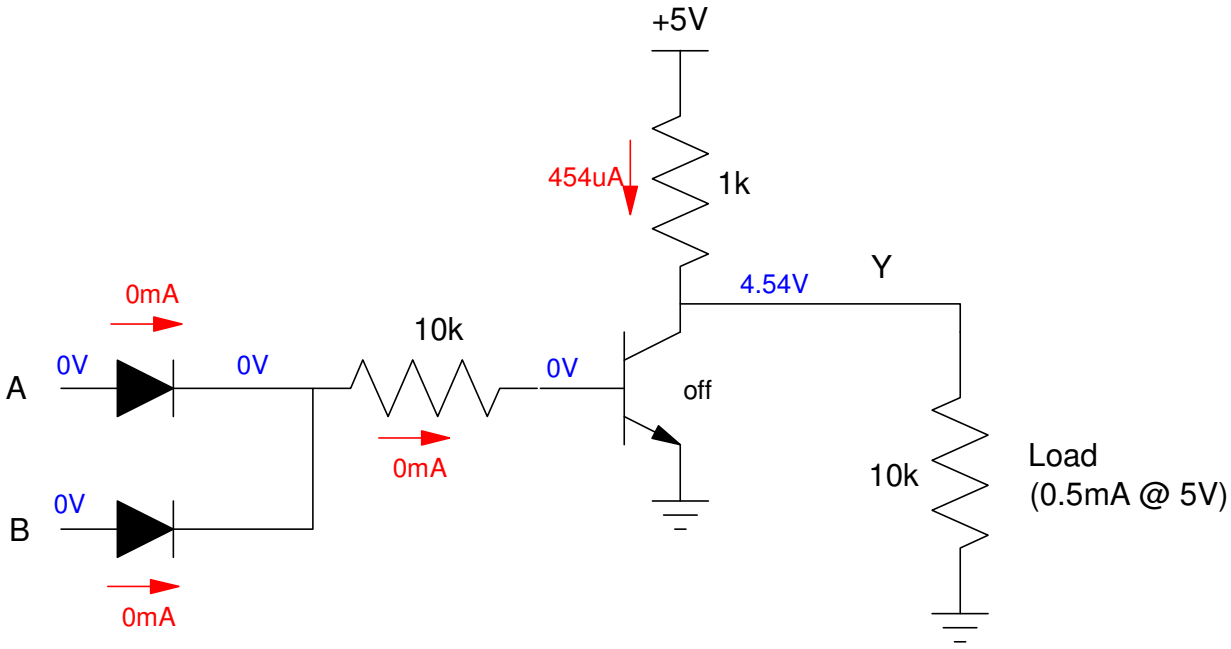
- Both diodes are off
- Transistor is off

By voltage division

$$Y = \left(\frac{10k}{10k+1k}\right)5V = 4.54V$$

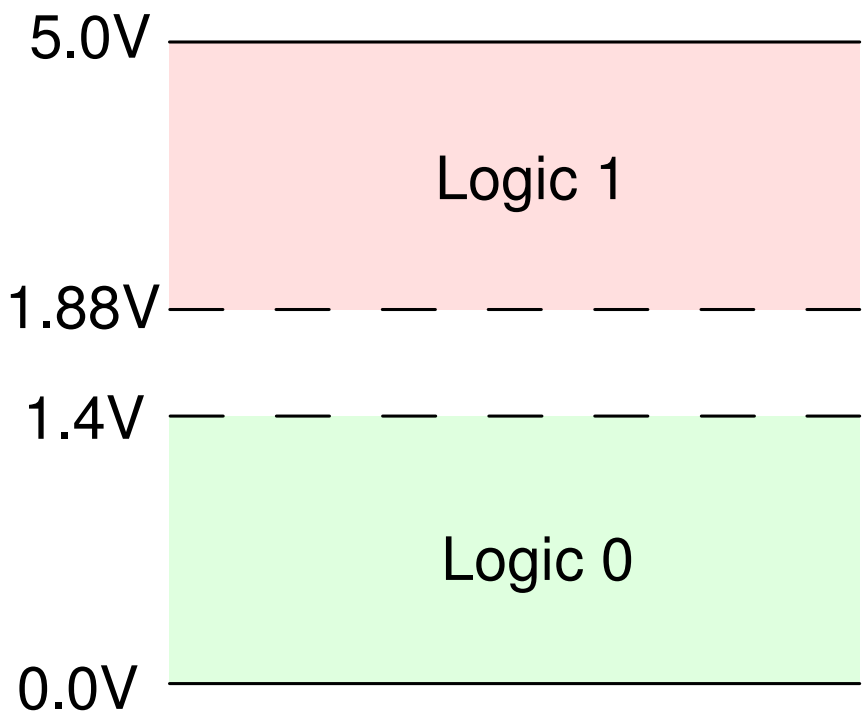
Va < 1.4V assures Ib = 0

Logic level 0: < 1.4V



Logic Levels

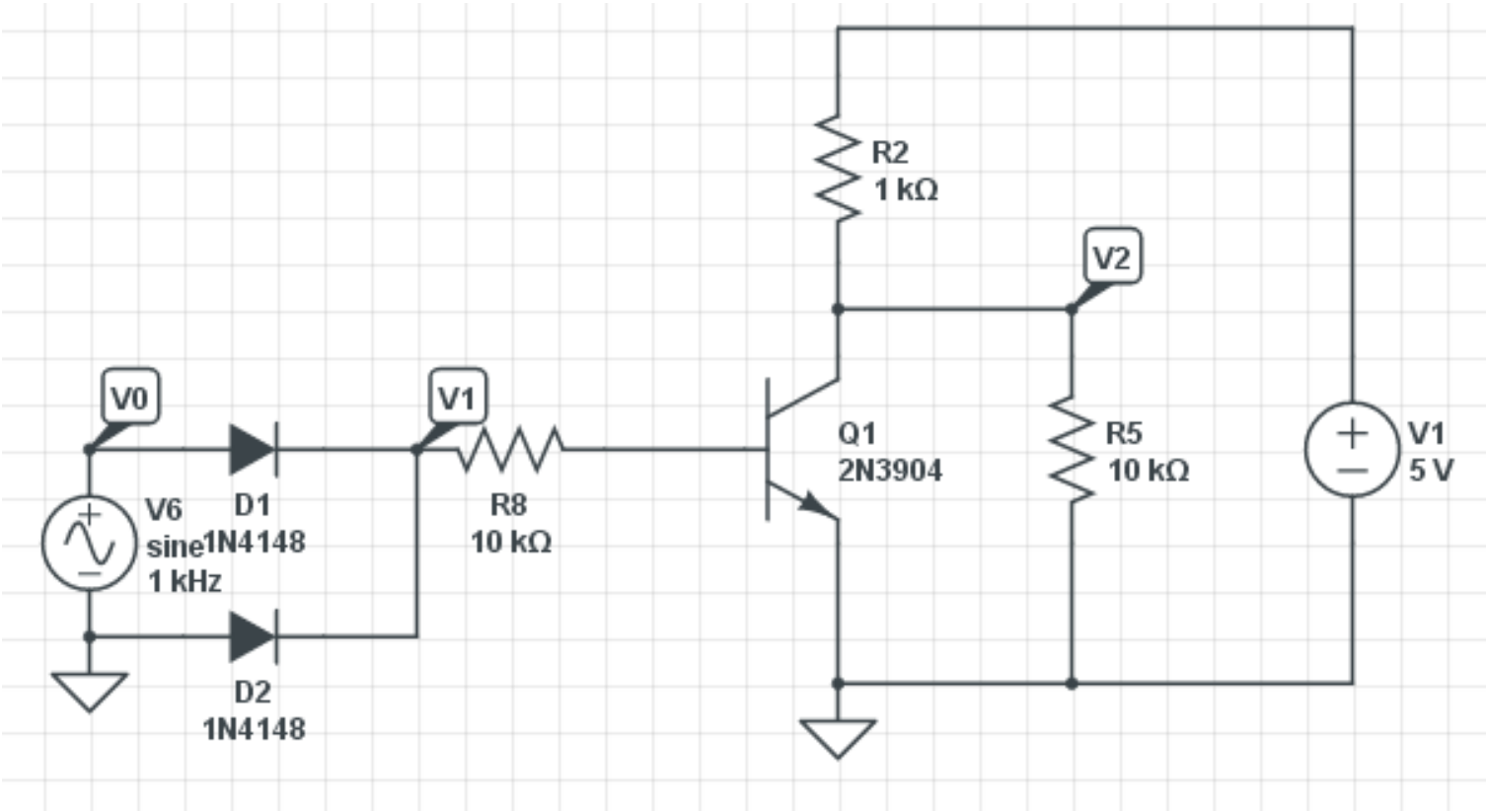
- Vin > 1.88V Transistor is saturated
- Vin < 1.40V Transistor is off



Logic Levels for a DTL NOR gate.

CircuitLab Simulation

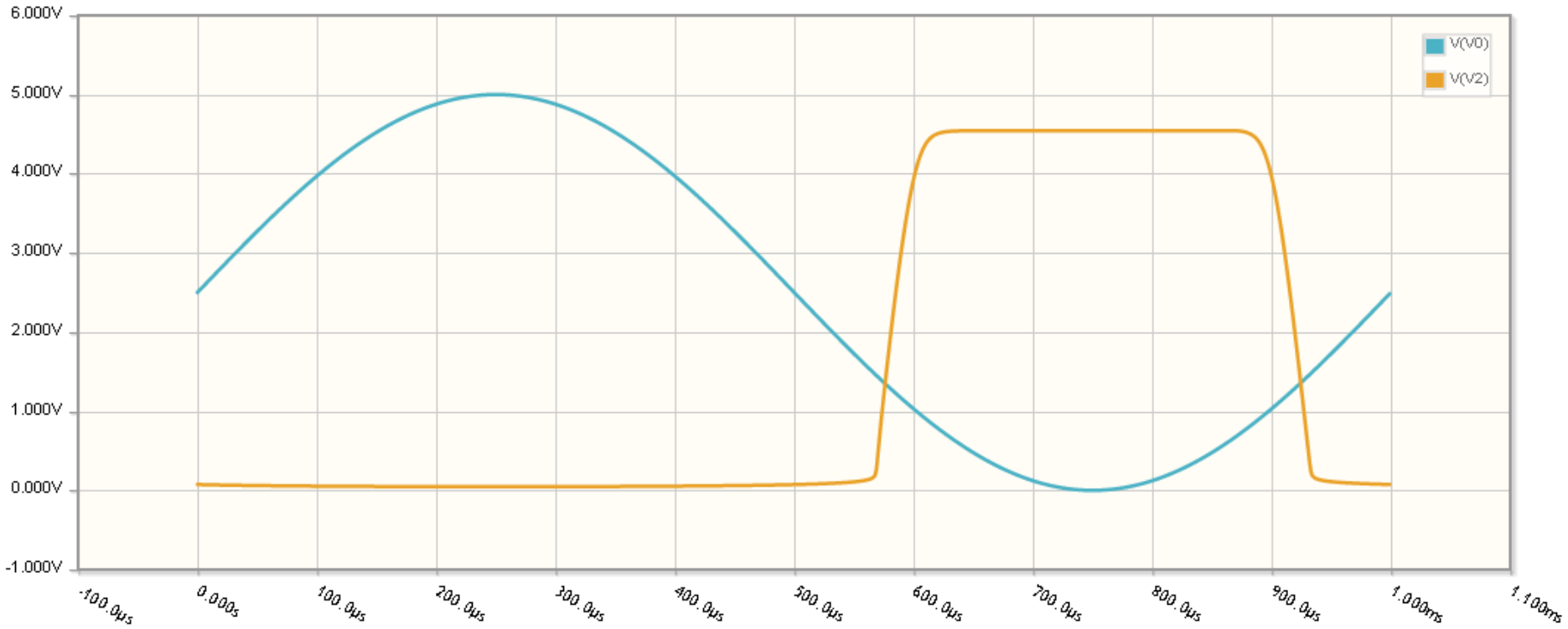
- B = 0V
- A = 0V .. 5V sine wave



DTL Circuit for determining logic level 1 and 0

DTL NOR Gate Logic Levels (experimental)

- Vin > 1.464V Saturated (Y < 200mV)
- Vin < 688mV Off (Y > 4.53V)



V0 (blue) and V2 (orange). The input is logic level 0 when V2 = 4.54V (Q1 is off)
Logic level 1 when V2 < 200mV (Q1 is saturated)

Fanout

- How many devices can you add?
- Each NOR gate draws 327uA

$$\left(\frac{5V-1.4V}{10k+1k}\right) = 327\mu A$$

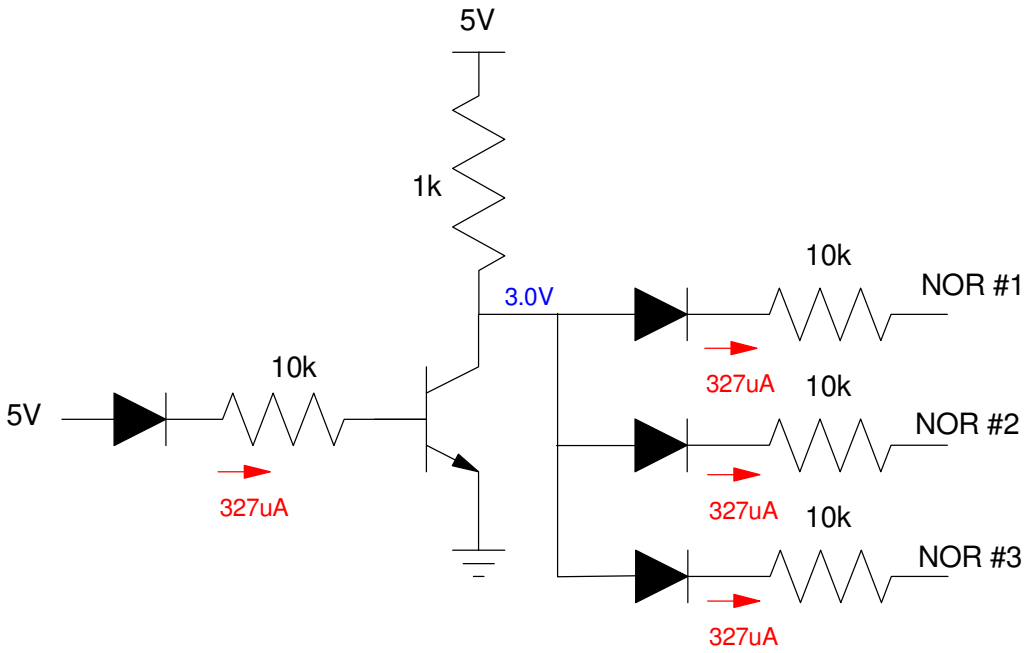
- With Rc = 1k, this is 327mV / gate.

For a 2V droop in Vc

$$N = \left(\frac{2V}{327mV/gate}\right) = 12.22\ gates$$

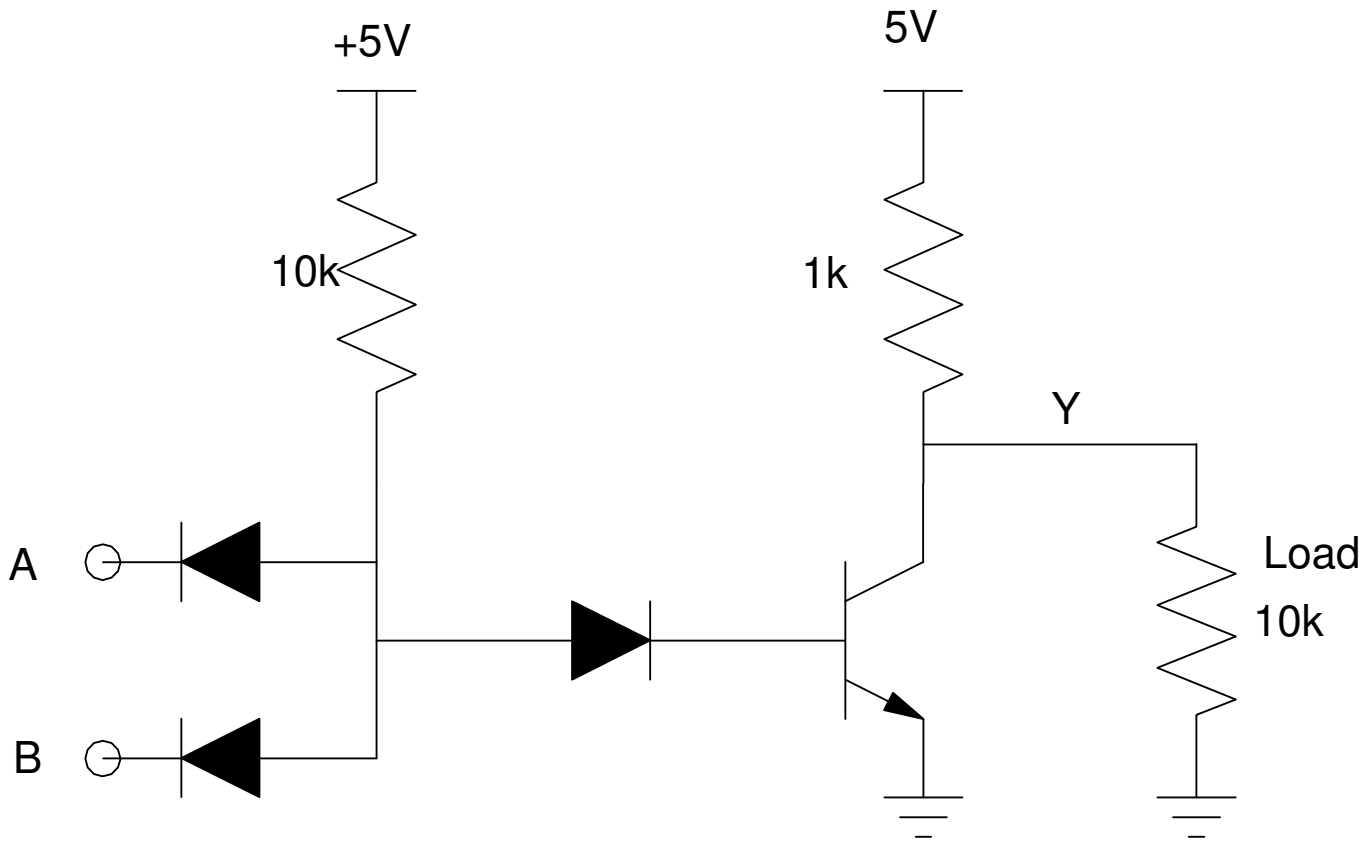
This gate has a fanout of twelve

- it can drive up to 12 similar gates



DTL NAND Gate:

Diodes arranged as a min() function creates a NAND gate.



DTL NAND gate

Case 1: Va = 5V, Vb = 0V

- Diode B is ON
- Transistor is off
- Y = 4.54V

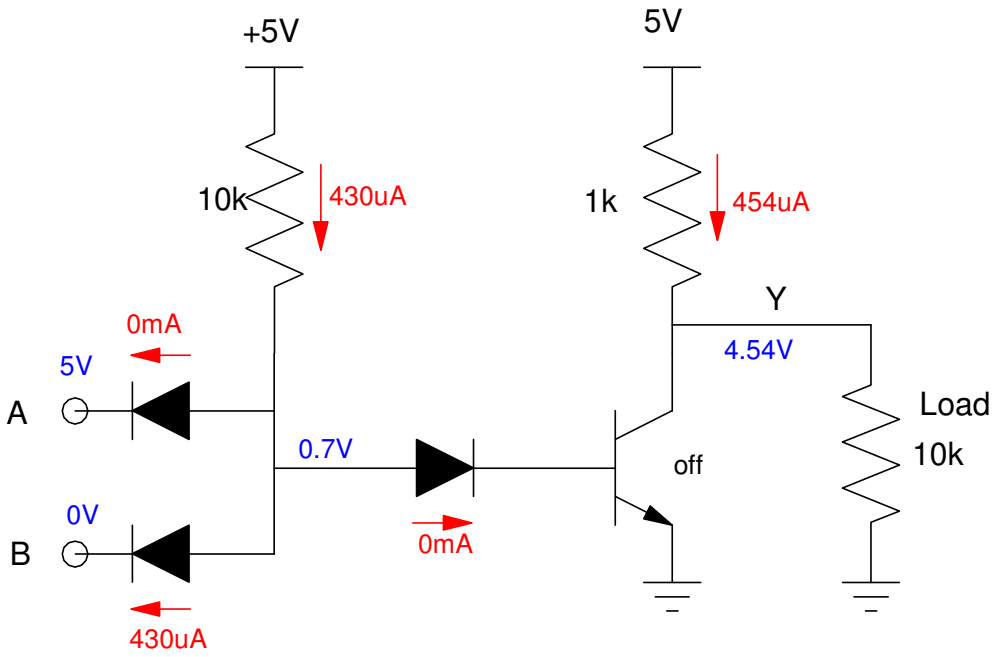
$$Y = \left(\frac{10k}{10k+1k}\right)5V = 4.54V$$

The same is true if either A or B is 0V:

- the transistor is off and Y = 4.54V.

Logic Level:

- Ib = 0 as long as Vb < 700mV

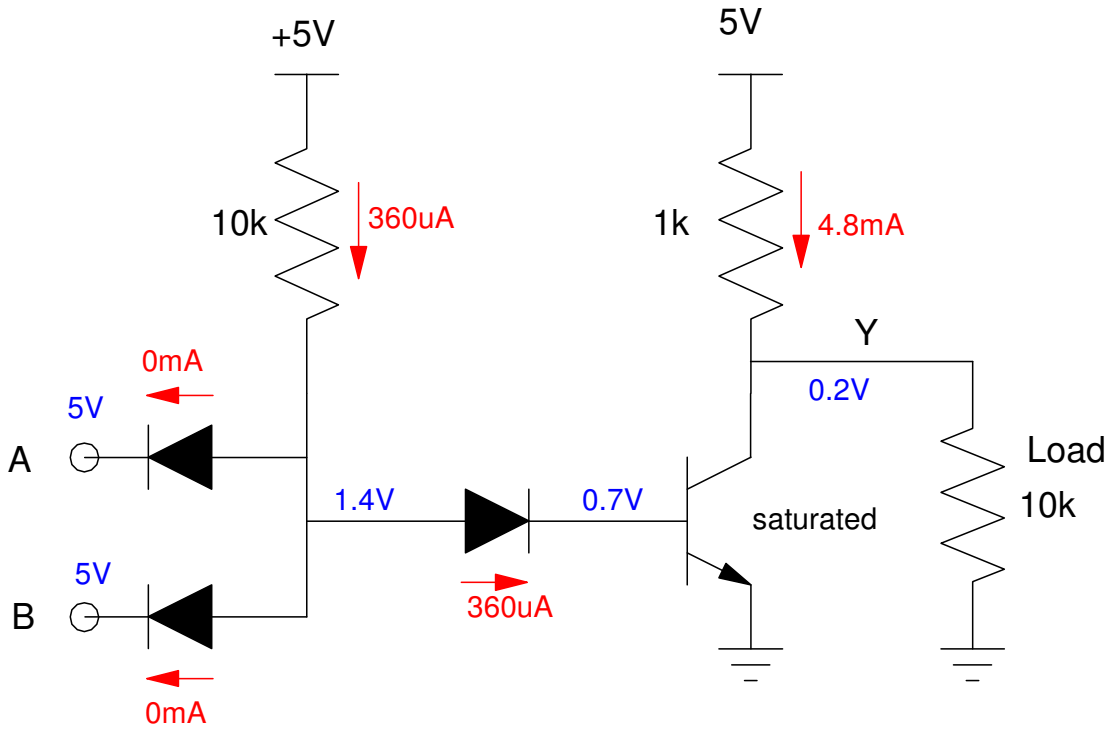


Case 2: Va = 5V, Vb = 5V

- Diode A and B are off
- Ib = 360uA
- $\beta I_b = 36mA$
- Transistor is saturated
- Y = 0.2V

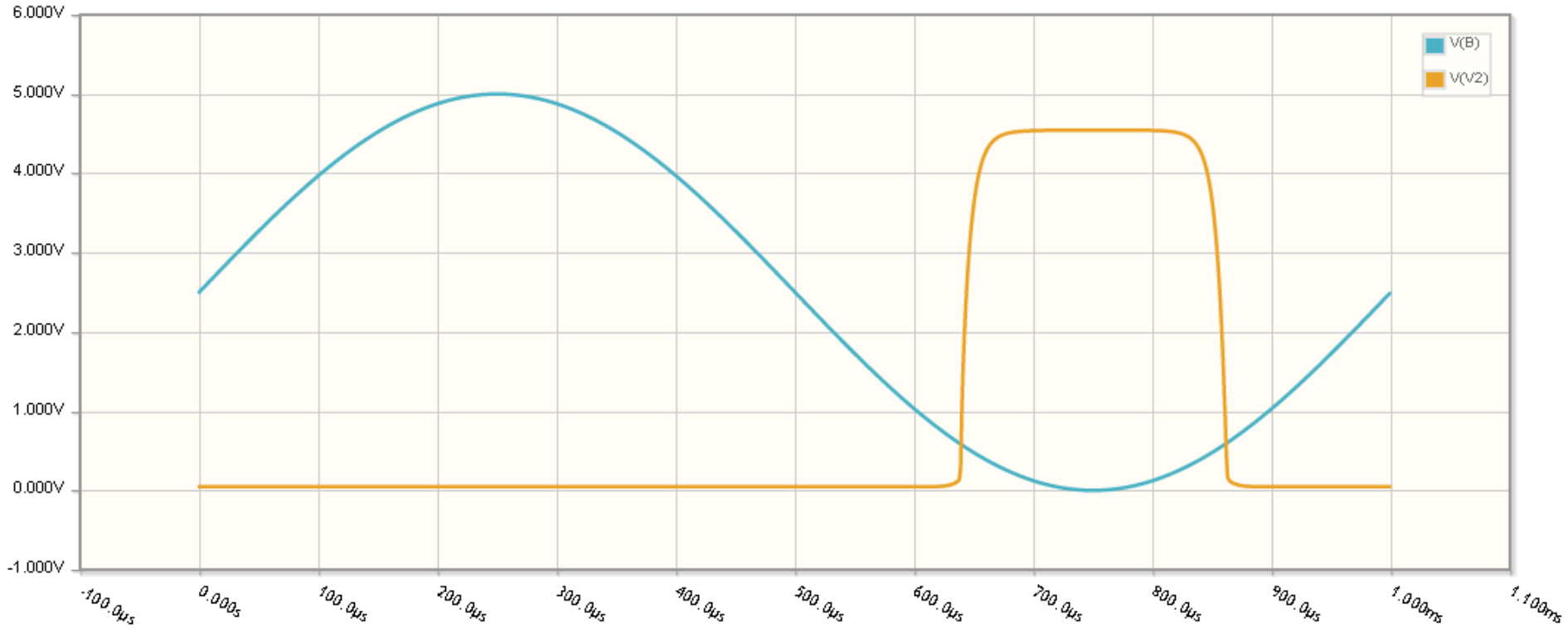
Logic Level:

- Ib = 360uA as long as Vb > 700mV



NAND Logic Levels

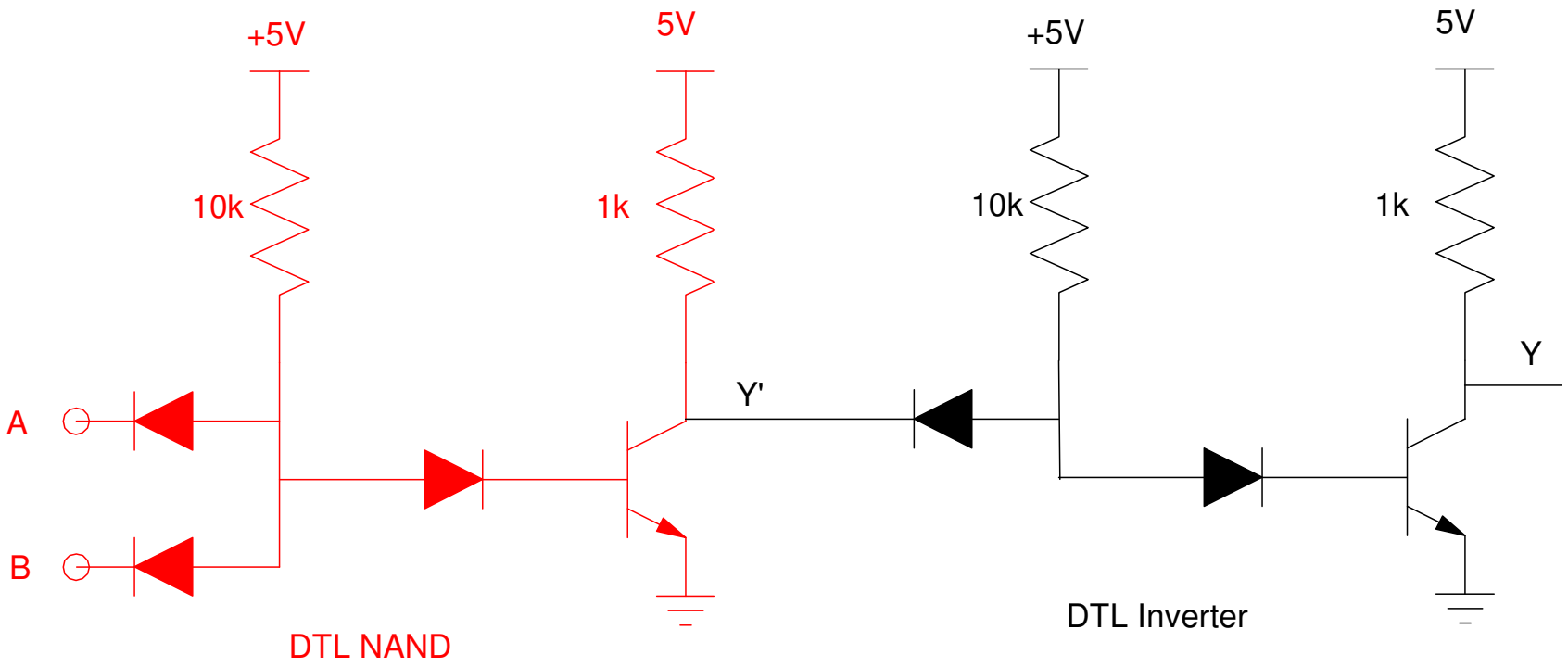
- Vin > 811mV Logic level 1 (transistor is saturated, Y < 50mV)
- Vin < 301mV Logic level 0 (transistor is off, Y > 4.53V)



Logic levels from Circuitlab. The transistor is saturated (logic level 0) when Vin > 800mV
The transistor is off (logic level 1) when Vin < 265mV

DTL AND gate.

- A single transistor creates a NAND or NOR gate
- Two transistors build an AND and OR gate

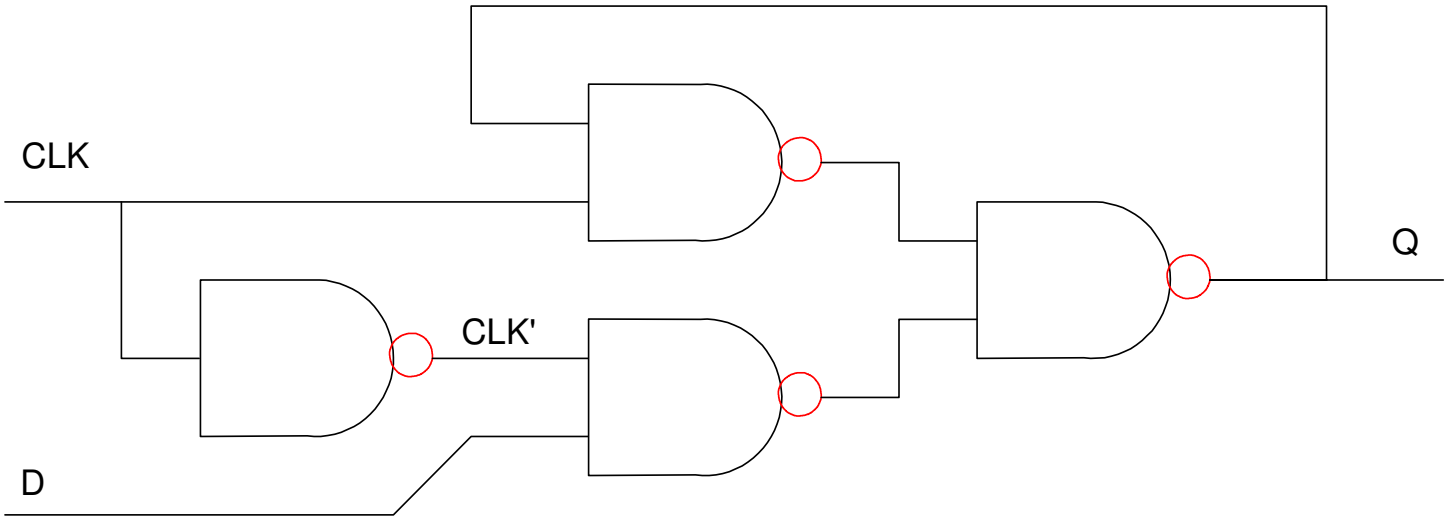


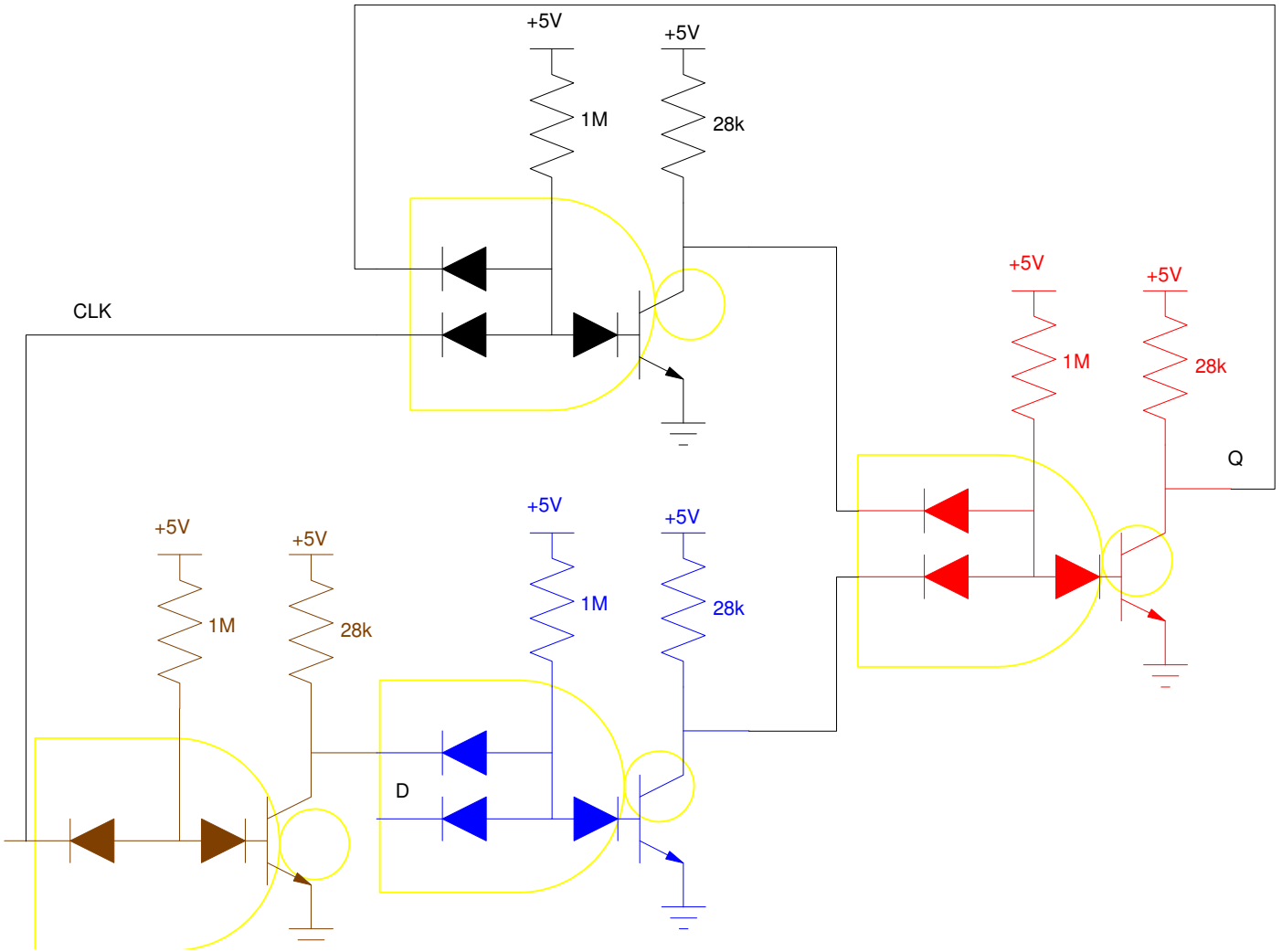
Two transistors are required to created a DTL AND gate.

D-Flip Flop Design with DTL Logic:

- NAND and NOR gates can build anything
- Example: D Flip Flop

$$Q = Q \cdot \overline{CLK} + CLK \cdot D$$

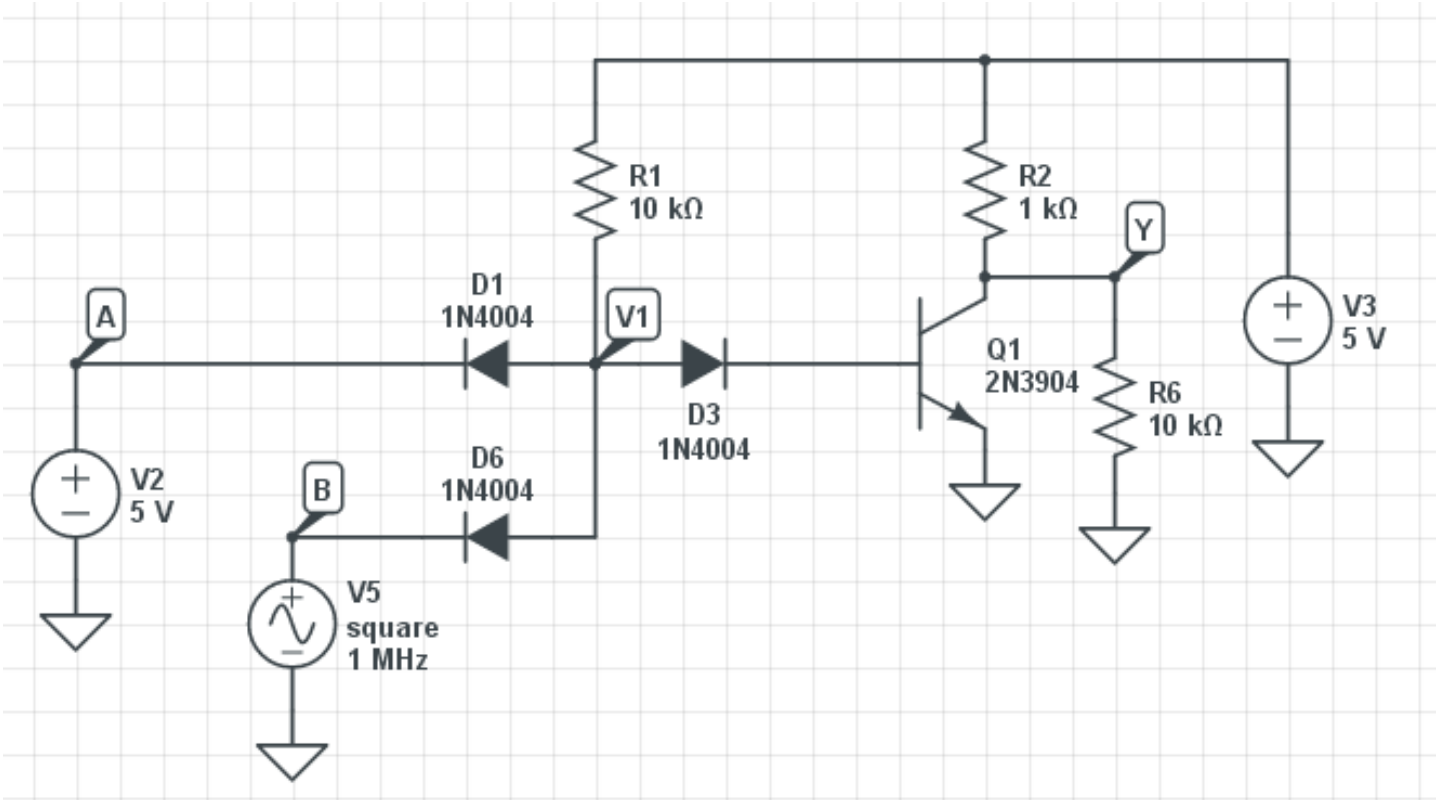



+5V
+5V
1M
28k
CLK
+5V
+5V
1M
28k
Q
+5V
+5V
1M
28k
D
+5V
+5V
1M
28k

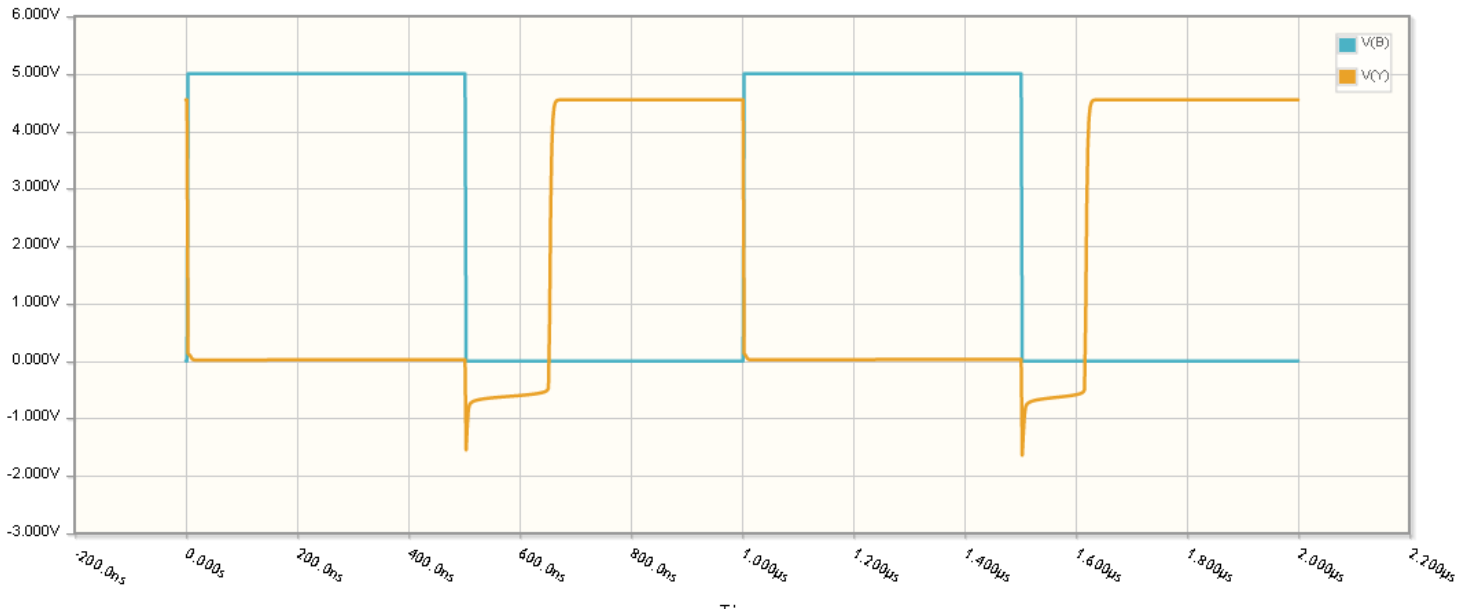
Frequency Limitations of DTL Logic

DTL logic has several problems that you can see in CircuitLab. Take for example a DTL NAND gate:

- If you clock the input at 1MHz, the output looks like the following:



DTL NAND gate. V5 is a 0V / 5V 1MHz square wave.



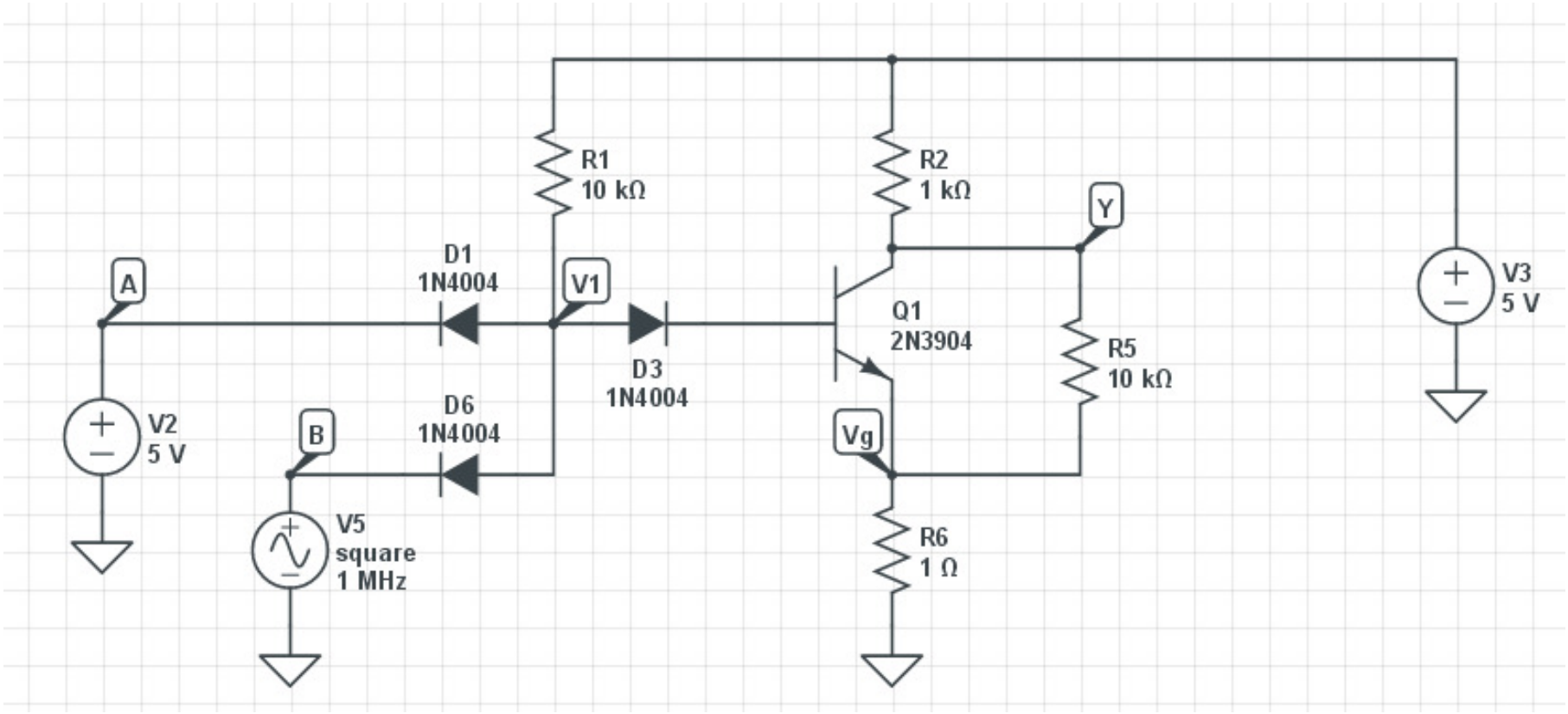
Limitation on clock speed with DTL Logic.

What this tells you is that it takes about 170ns for the DTL circuit to go from logic level 0 to logic level 1. This is due to the inherent capacitance of the diodes. What this means is

- The maximum clock frequency of DTL logic is about 1MHz.
- If you want to clock it faster, you need to get rid of the diodes (i.e. use TTL logic, presented in the next lecture).

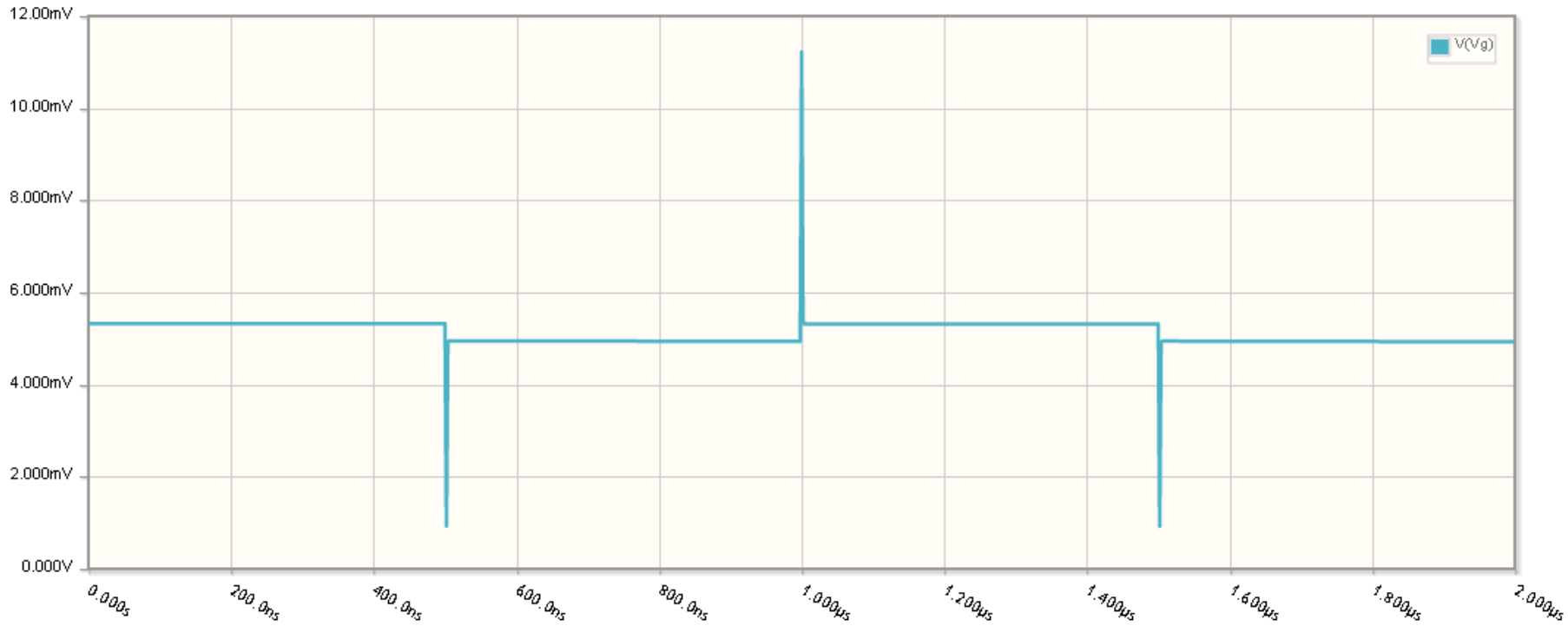
Current Spikes with DTL logic

One problem with digital logic is it produces spikes in current. To measure this, add a 1 Ohm resistor in series with ground.



DTL NAND gate with R6 added so that you can measure current.

The 1 Ohm resistor then acts as a current sensor: 1V = 1A. The current (i.e. voltage) produced for a 1MHz square wave input is as follows:



Vg vs. time. Note that current spikes happen whenever the output changes logic levels.

What this means is

- Any time you have digital logic, you will have spikes in current.
- To reduce the impact of these spikes, capacitors are often scattered across a circuit board with digital logic.
- If your circuit includes analog electronics, keep the power for the digital section separate from the power to the analog section. Otherwise, the digital section will add noise to the analog section.

Summary

With diodes, you can build min / max functions

- Heart of fuzzy logic
- But, you lose 0.7V for each stage

DTL logic adds a transistor at the output

- Cleans up the logic levels
- Increases the output current capability

But, the diode slows down the response time

- Diodes are inherently capacitors
- RC time constant limits the maximum clock frequency