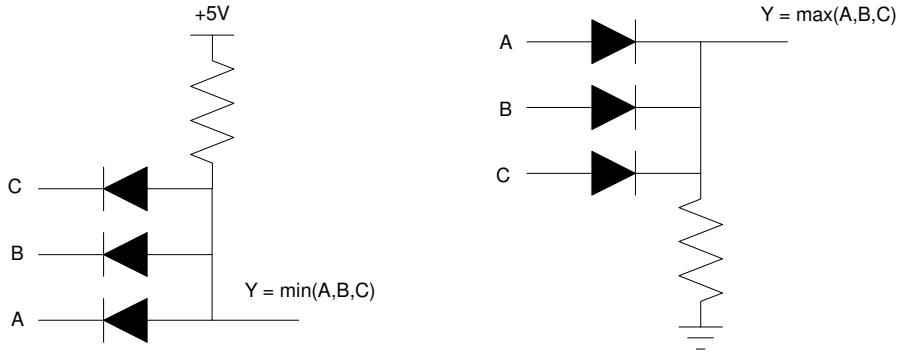
Diode Transistor Logic (DTL)

Logic AND operates sort of like a minimum function. The minimum voltage of all inputs is zero if any of them are zero. It's 5V only if they all are 5V.

Logic OR operates sort of like a maximum function. The maximum voltage of all inputs is 5V if any of them is 5V. It's 0V only they all are 0V.

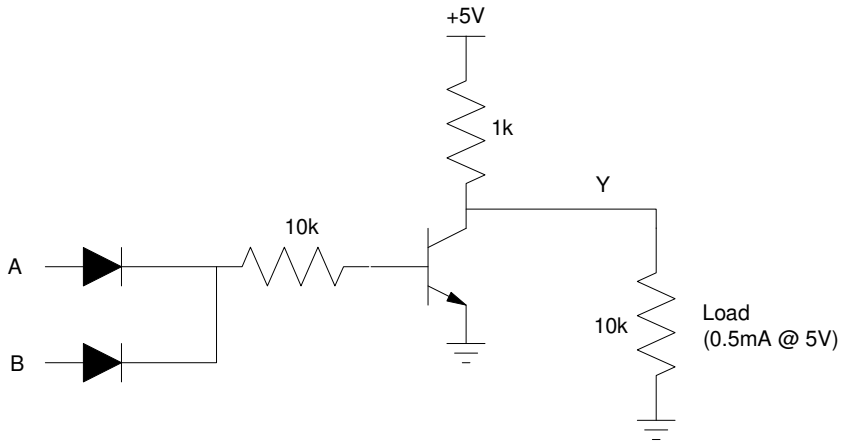
You can use the previous diode circuit for a min or max function, likewise:



A problem with these circuits is the diode has a 0.7V drop across it. Likewise, if you cascade a bunch of these together, you eventually run out of voltage. To bring the output back to 5V, use a transistor as a switch: when the output is high, turn on the diode. If there isn't enough voltage, the transistor turns off:

DTL NOR Gate

Consider the following DTL NOR gait. Determine the voltages and currents:



DTL NOR gate: a max(A,B) function is coupled with a transistor to return the logic levels to 0V / 5V

Case 1: A = 5V, B = 0V. If either A or B is 5V, you get current flow - which saturates the transistor. To keep it simple, assume A = 5V and B = 0V.

The current from Va passes through two diodes, dropping 1.4V. The remaining 3.6V is across the 10k resistor, resulting in

$$I_b = \left(\frac{5V-1.4V}{10k}\right) = 360\mu A$$

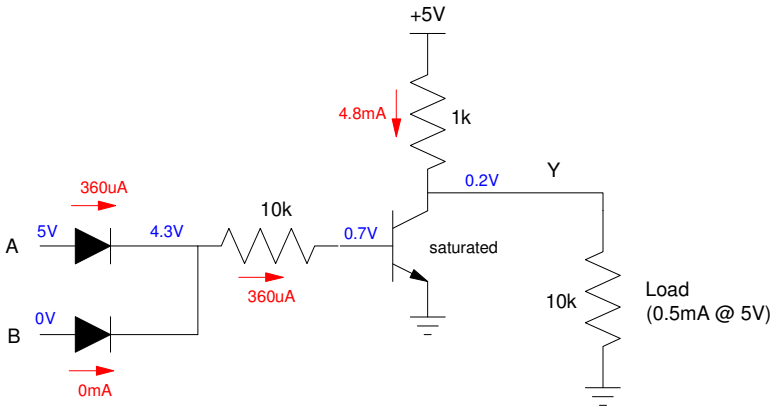
Assuming β=100, this allows up to 36mA to flow through the transistor:

$$\beta I_b = 36mA$$

The maximum current possible due to the 1k resistor is 4.8mA

$$\max(I_c) = \left(\frac{5V-0.2V}{1k}\right) = 4.8mA$$

so the transistor is saturated. The resulting voltages and currents are then as follows:



DTl NOR gate: Voltages and Currents for A = 5V, B = 0V

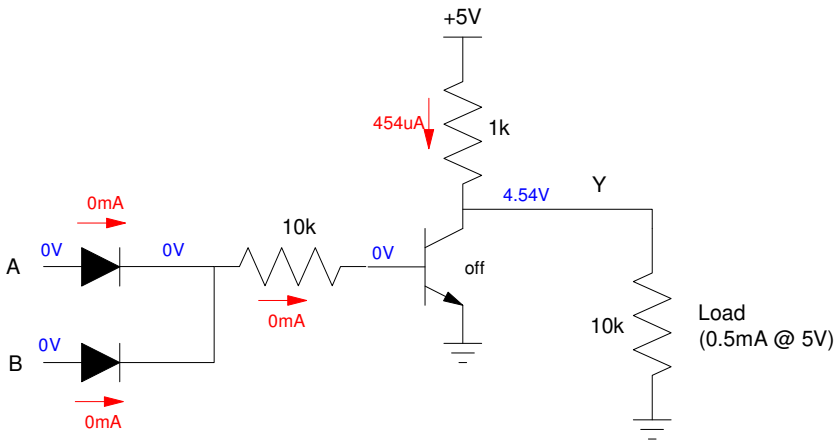
Note that as long as the transistor is saturated, the output is logic 0. To saturate the transistor, you need at least 48uA flowing in the base. The lowest that Va can be is then

$$\left(\frac{V_A-1.4V}{10k}\right) > 48\mu A$$

$$V_A > 1.88V$$

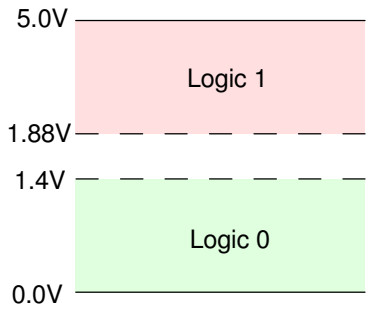
Case 2: Va = Vb = 0V. In this case, the base current will be zero. This turns off the transistor, resulting in Y from voltage division being

$$Y = \left(\frac{10k}{10k+1k}\right)5V = 4.54V$$



DTl NOR gate: Voltages and currents for Va = Vb = 0V

Note that as long as Va < 1.4V, the base diode will be turned off. This results in logic 0 being anything less than 1.4V



Logic Levels for a DTL NOR gate.

In CircuitLab, you can check these logic levels. Let

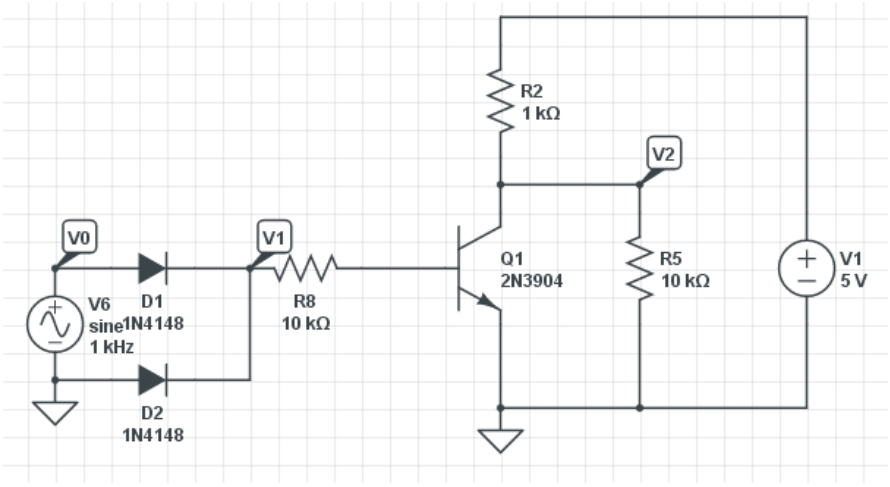
- B = 0V
- A = 0V .. 5V sine wave

and plot Y.

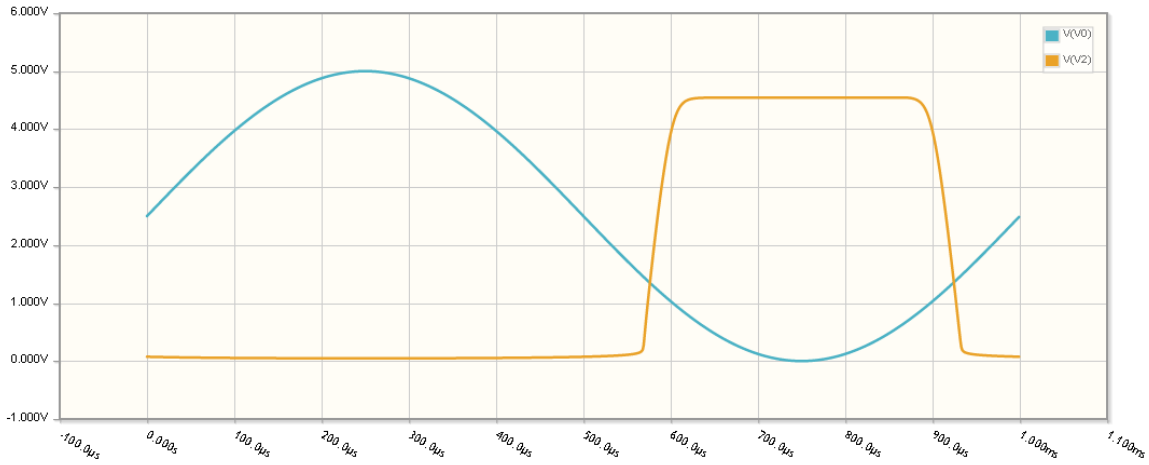
- When Y = 0.2V, the transistor is saturated and you're at logic level 0
- When Y = 4.54V, the transistor is off and you're at logic level 1
- In-between, the transistor is in the active region (bad).

This results in

- Vin > 1.464V Saturated (Y < 200mV)
- Vin < 688mV Off (Y > 4.53V)



DTL Circuit for determining logic level 1 and 0



V0 (blue) and V2 (orange). The input is logic level 0 when V2 = 4.54V (Q1 is off)
Logic level 1 when V2 < 200mV (Q1 is saturated)

Fanout: Each gate draws as much as 360uA. As you draw more and more current, the voltage at the output drops. If it drops below 1.88V, you're no longer at logic level 1. Fanout is how many gates you can drive with a single NOR gate.

Each NOR gate draws 327uA:

$$\left(\frac{5V-1.4V}{10k+1k}\right) = 327\mu A$$

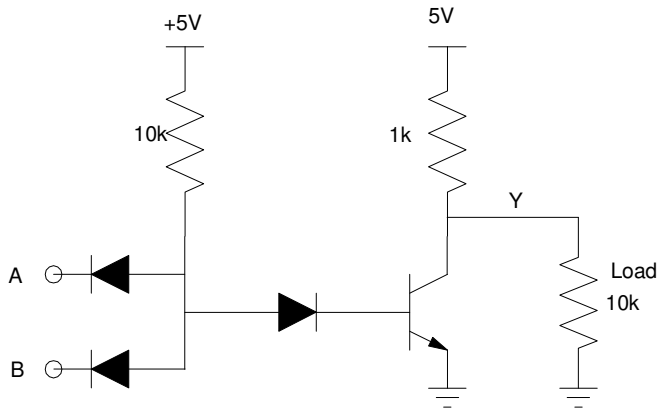
With Rc = 1k, this corresponds to 327mV / gate. If Vc can only drop 2V, you can drive 12 gates

$$N = \left(\frac{2V}{327mV/gate}\right) = 12.22\ gates$$

This gate has a fanout of eight (it can drive up to 8 similar gates).

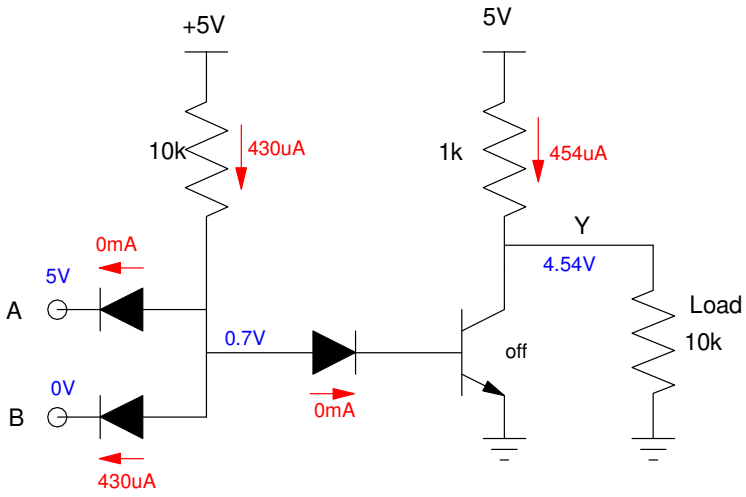
DTL NAND Gate:

Diodes arranged as a min() function creates a NAND gate.



DTL NAND gate

Case 1: Va = 5V, Vb = 0V



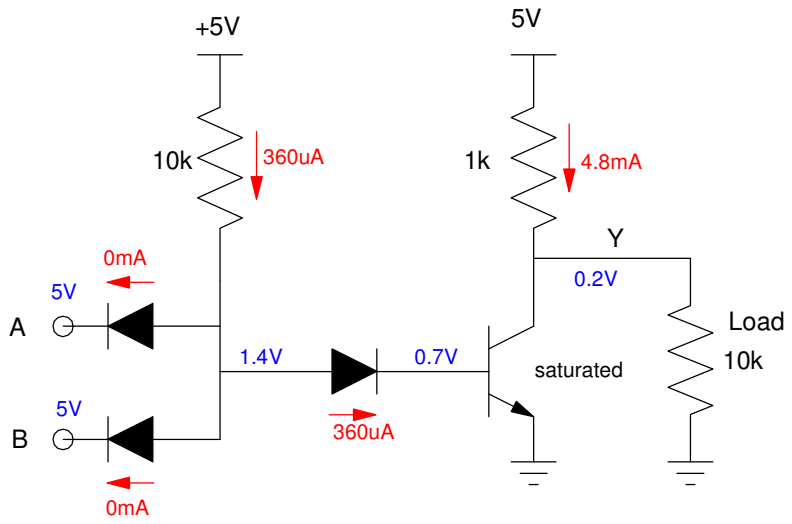
DTL NAND gate with Va = 5V, Vb = 0V.

The diode tied to 0V turns on, making the voltage on the right 0.7V. You need 1.4V to turn on the base diode, so Ib = 0mA. This turns the transistor off. The voltage at Y is then

$$Y = \left(\frac{10k}{10k+1k}\right)5V = 4.54V$$

The same is true if either A or B is 0V: the transistor is off and Y = 4.54V.

Case 2: Va = 5V, Vb = 5V



DTL NAND gate with Va = Vb = 5V.

Both diodes tied to A and B are off. The current from the 5V source then flows right through the base of the transistor. This results in 1.4V at the bottom of the 10k resistor and 360uA flowing into the base of the transistor.

360uA allows up to 36mA to flow in the transistor. The maximum current this transistor can sink is 4.8mA however

$$\max(I_c) = \left(\frac{5V - 0.2V}{1k}\right) = 4.8mA$$

so the transistor is saturated. Y = 0.2V.

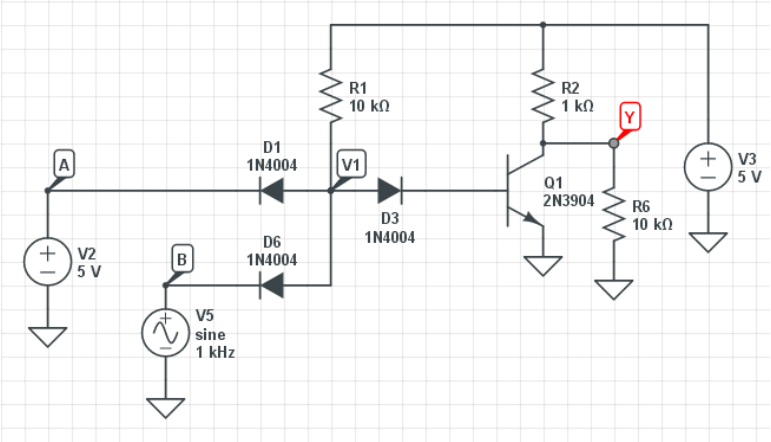
NAND Logic Levels

Using CircuitLab, you can determine the logic levels at the input.

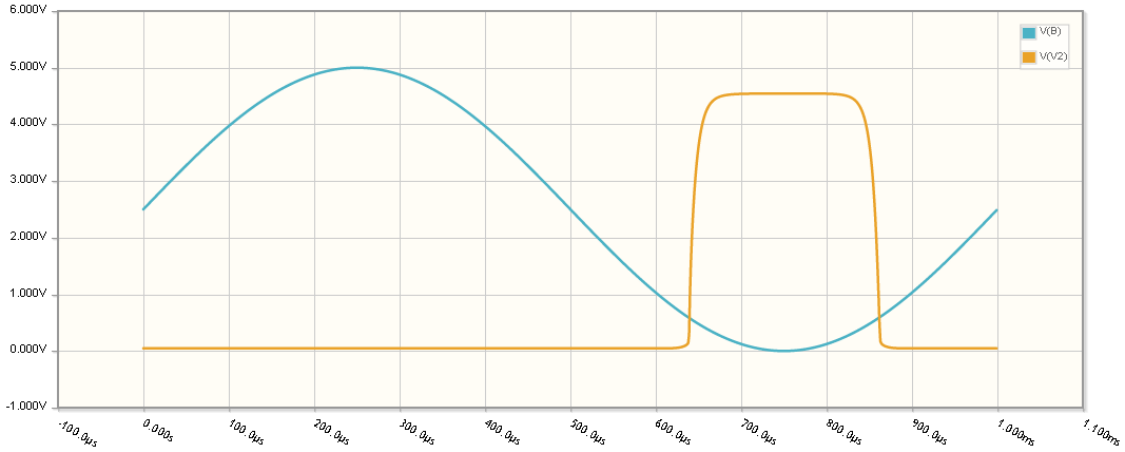
- If the transistor is saturated, the input is logic level 1
- If the transistor is off, the input is logic level 0

This results in

- Vin > 811mV Logic level 1 (transistor is saturated, Y < 50mV)
- Vin < 301mV Logic level 0 (transistor is off, Y > 4.53V)



DTl NAND gate in CircuitLab. B is a sine wave so you can determine logic level 0 and 1

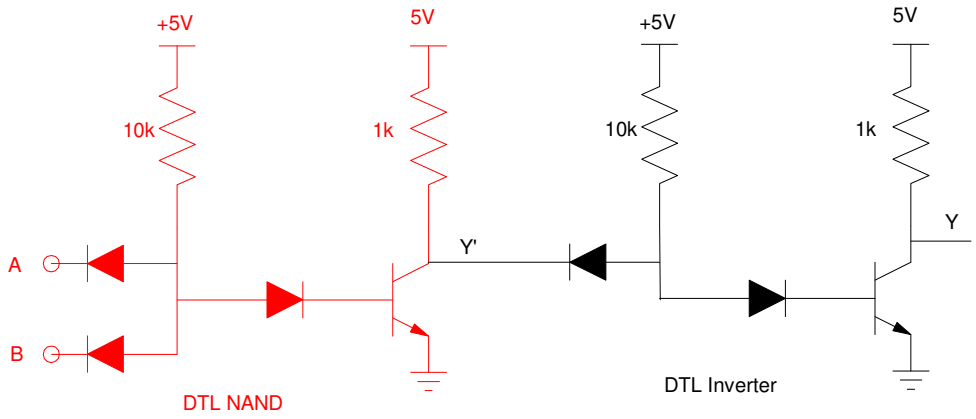


Logic levels from Circuitlab. The transistor is saturated (logic level 0) when Vin > 800mV
The transistor is off (logic level 1) when Vin < 265mV

DTL AND gate.

A single transistor creates a NAND or NOR gate. To build an AND gate, you need two transistors. That's twice as expensive - hence we normally use NAND or NOR.

It doesn't really matter which one you use: both NAND and NOR use the same number of transistors (one):



Two transistors are required to created a DTL AND gate.

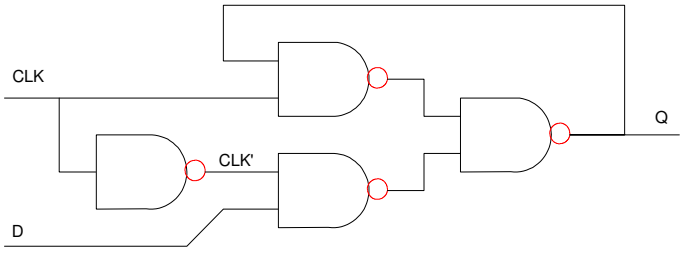
D-Flip Flop Design with DTL Logic:

In ECE 275, you learned how to combine NAND and NOR gates to create different logic functions. At the transistor level, just replace the NAND and NOR gate with their transistor circuit.

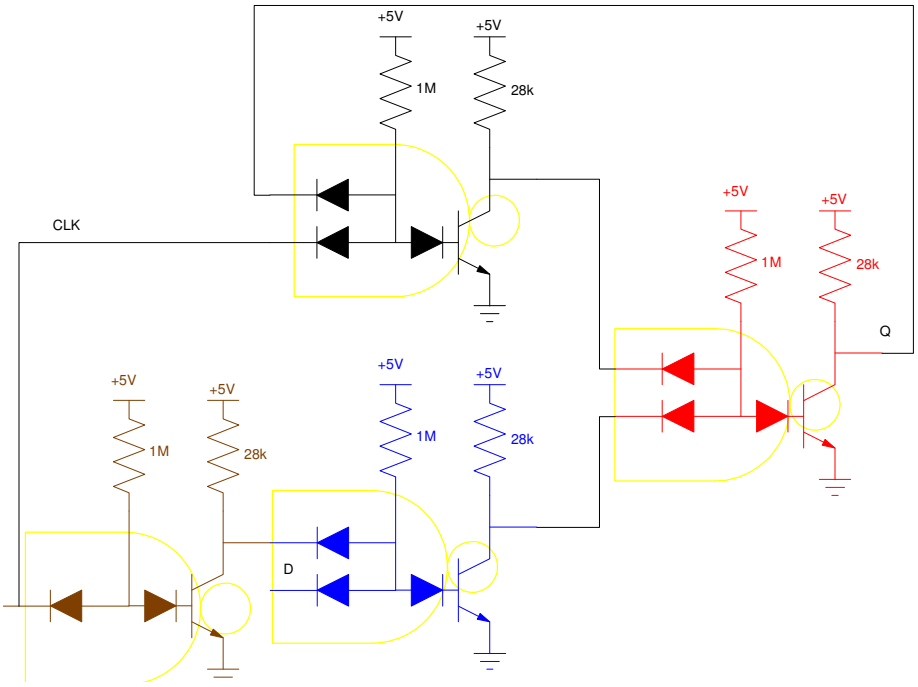
For example, build a D flip-flop at the transistor level. The logic for a D flip-flop is

$$Q = Q \cdot \overline{CLK} + CLK \cdot D$$

Throwing in a double negative on the output of the AND gates converts these to NAND and NOT-OR (also a NAND). CLK' comes from another NAND, so



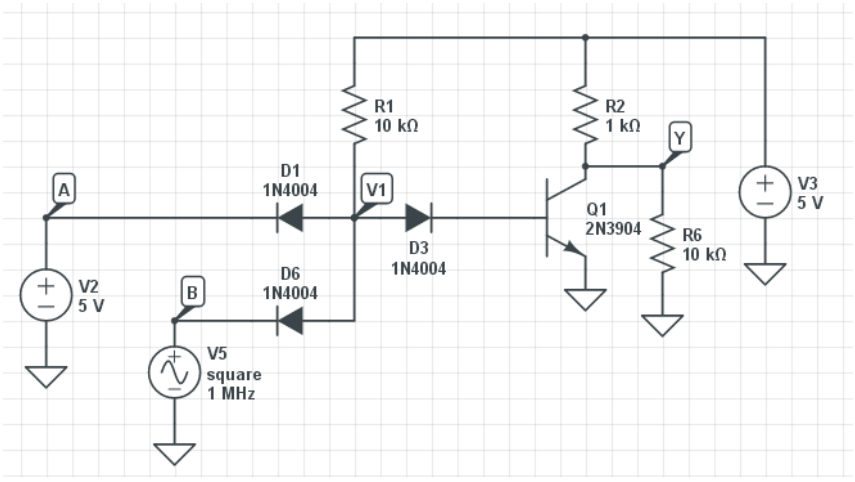
At the transistor level this is then:



D flip flop with DTL logic. Each NAND gate is shown in a different color

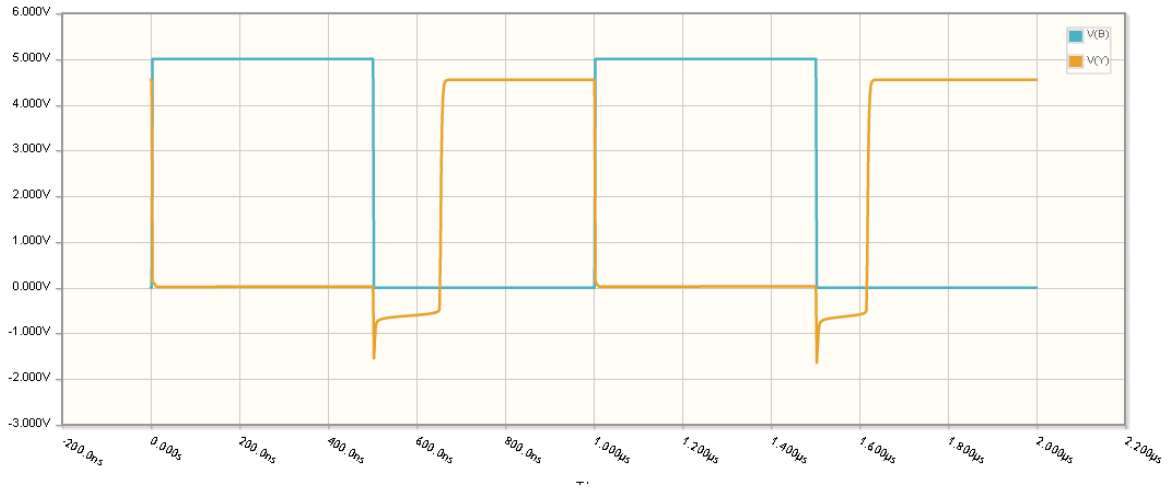
Frequency Limitations of DTL Logic

DTL logic has several problems that you can see in CircuitLab. Take for example a DTL NAND gate:



DTL NAND gate. V5 is a 0V / 5V 1MHz square wave.

If you clock the input at 1MHz, the output looks like the following:



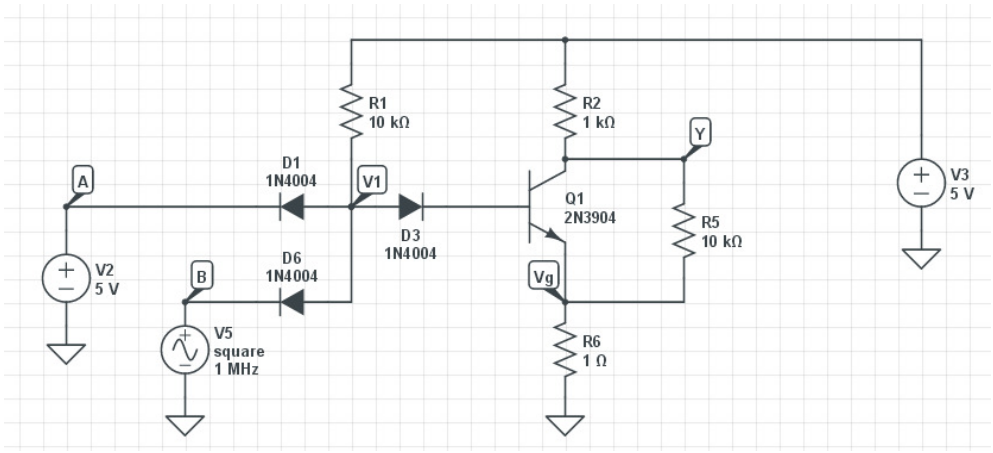
Limitation on clock speed with DTL Logic.

What this tells you is that it takes about 170ns for the DTL circuit to go from logic level 0 to logic level 1. This is due to the inherent capacitance of the diodes. What this means is

- The maximum clock frequency of DTL logic is about 1MHz.
- If you want to clock it faster, you need to get rid of the diodes (i.e. use TTL logic, presented in the next lecture).

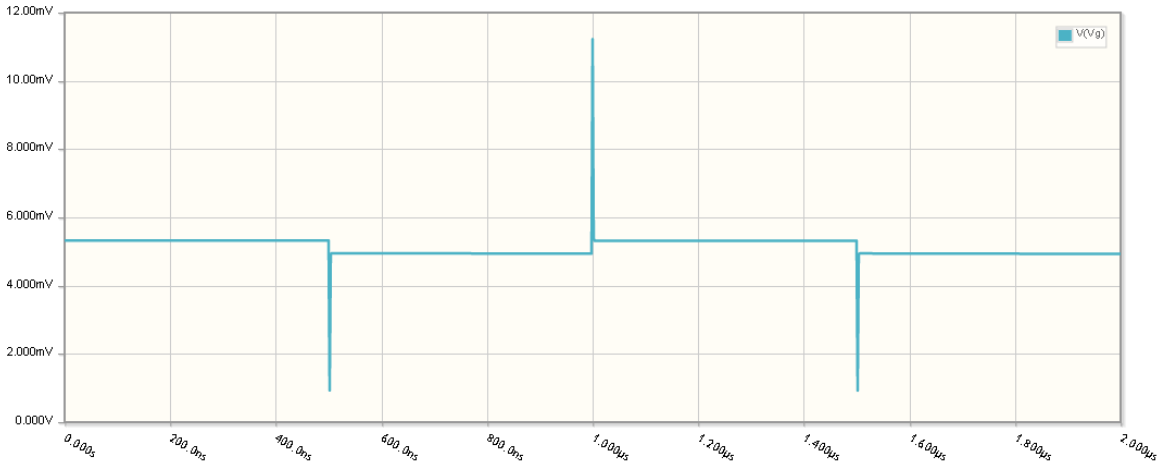
Current Spikes with DTL logic

One problem with digital logic is it produces spikes in current. To measure this, add a 1 Ohm resistor in series with ground.



DTL NAND gate with R6 added so that you can measure current.

The 1 Ohm resistor then acts as a current sensor: 1V = 1A. The current (i.e. voltage) produced for a 1MHz square wave input is as follows:



Vg vs. time. Note that current spikes happen whenever the output changes logic levels.

What this means is

- Any time you have digital logic, you will have spikes in current.
- To reduce the impact of these spikes, capacitors are often scattered across a circuit board with digital logic.
- If your circuit includes analog electronics, keep the power for the digital section separate from the power to the analog section. Otherwise, the digital section will add noise to the analog section.