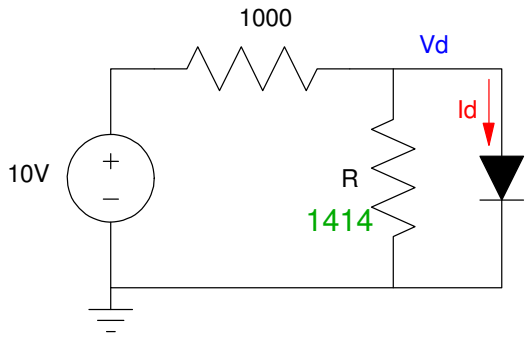
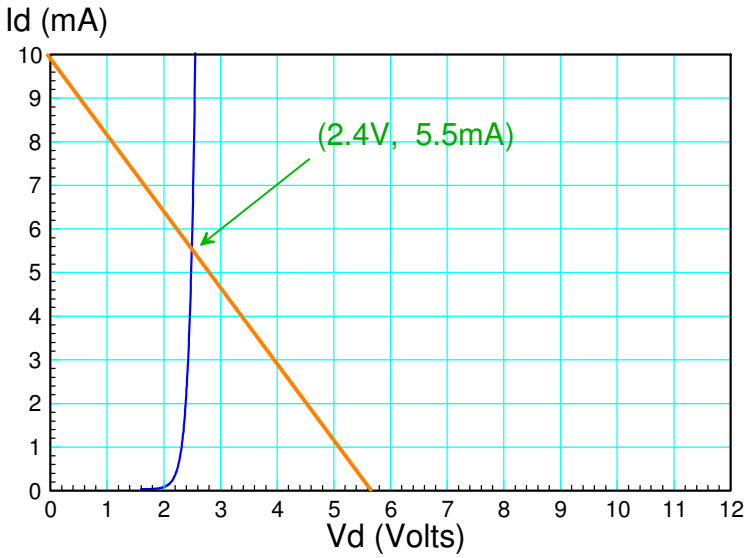
ECE 320 - Final (pt 1) - Name _____

Semiconductors & Diodes

1) Load Lines: Assume the VI characteristics for the diode is as shown in the graph. Draw the load line for the following circuit and determine Id and Vd. Assume R = 900 + 100*(your birth month) + (your birth date).

R 900 + 100*mo + day	Load Line x-intercept (volts)	Load Line y-intercept (mA)	Vd Volts	Id mA
1414	**5.857V**	**10.0mA**	**2.4V**	**5.5mA**





x-intercept (Id = 0)

$$V_d = \left(\frac{1414}{1414+1000}\right) 10V = 5.857V$$

y-intercept (Vd = 0)

$$I_d = \left(\frac{10V}{1000\Omega}\right) = 10mA$$

2) Nonlinear equations: Diode circuit

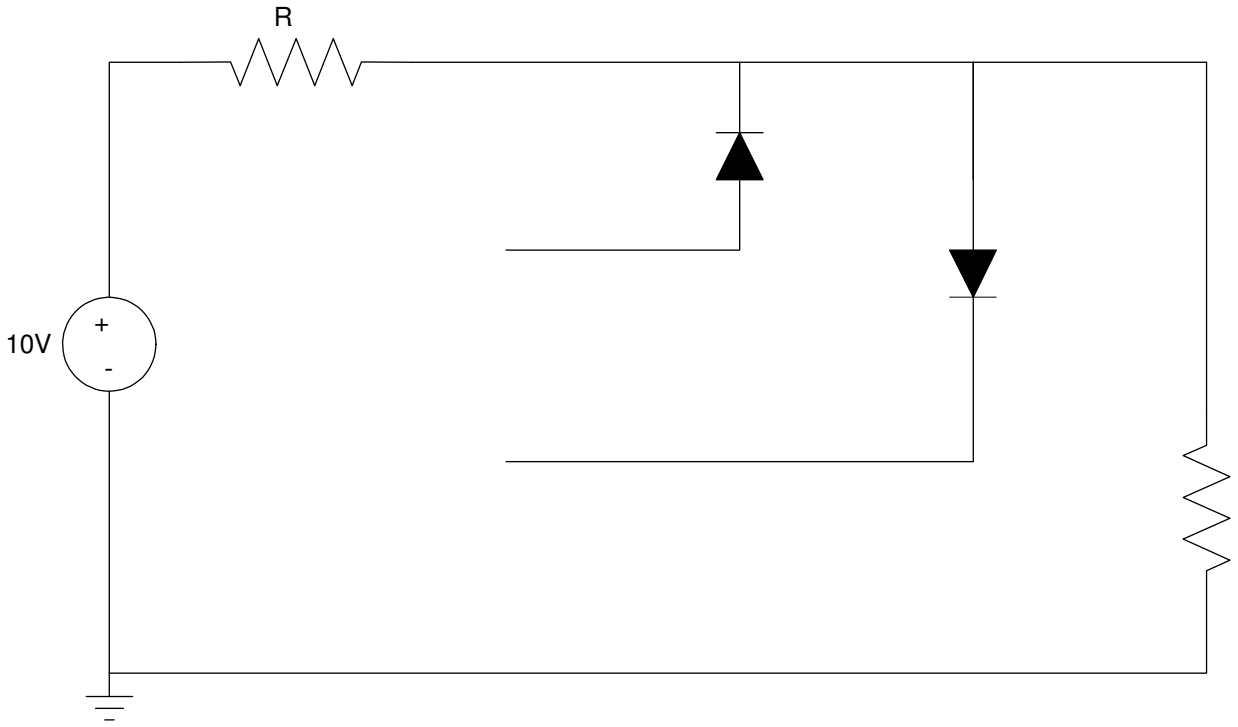
Assume the VI characteristics for the diodes shown below are

$$V_d = 0.038 \ln (10^{11} \cdot I_d + 1) \qquad I_d = 10^{-11} \cdot$$

3) Ideal Silicon Diodes. Assume the diodes in this circuit are ideal silicon diodes:

- Vd = 0.7V Id > 0
- Id = 0 Vd < 0.7V
- R = 900 + 100*(your birth month) + (birth date).

R 900 + 100*mo + day	Id1	Id2	Id3
1414	**0**	**1.578mA**	**0**
V1	V2	V3	V4
7.571V	**7.291V**	**6.871V**	**0V**

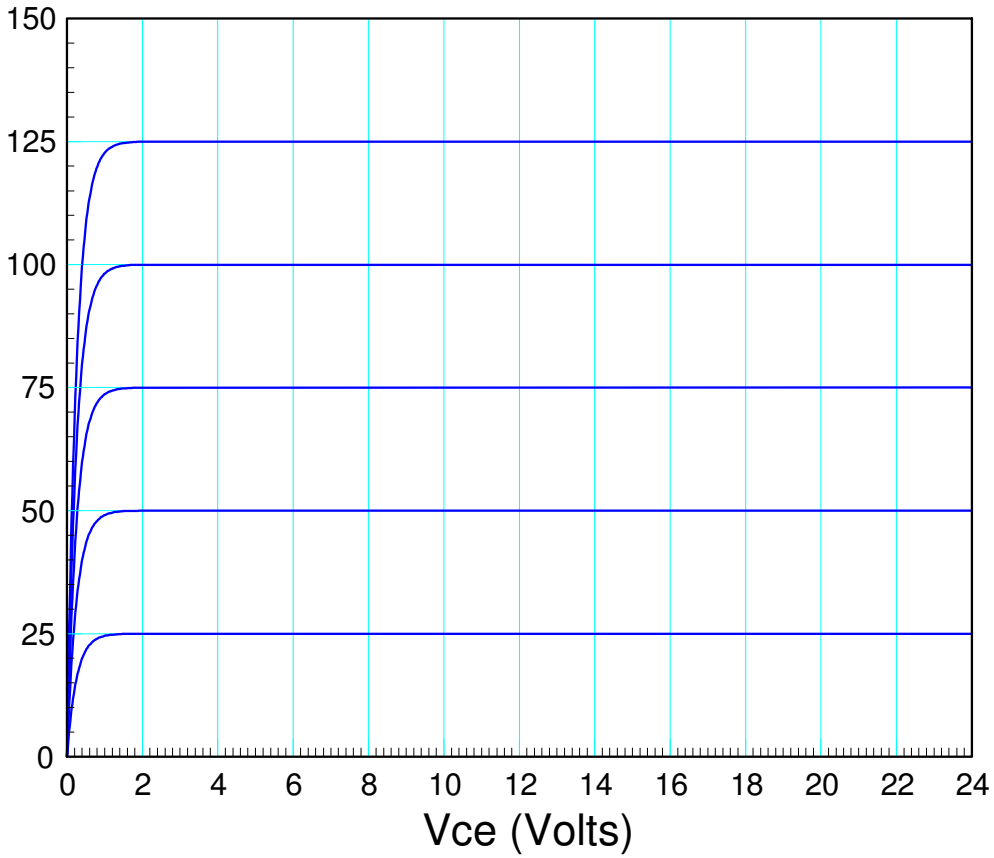


ECE 320 - Final (pt 2) - Name _____

Transistors and Mosfets

6) Determine the current gain, β. Also draw the load line and determine the operating point when Vin = 5V

R 900 + 100*Mo + Day	Current Gain hfe = beta	Load Line x-intercept (Volts)	Load Line y-intercept (mA)	Vce Vin = 5V	Ic Vin = 5V
1414	**25**	**20V**	**133.3mA**	**8.596V**	**76.025mA**

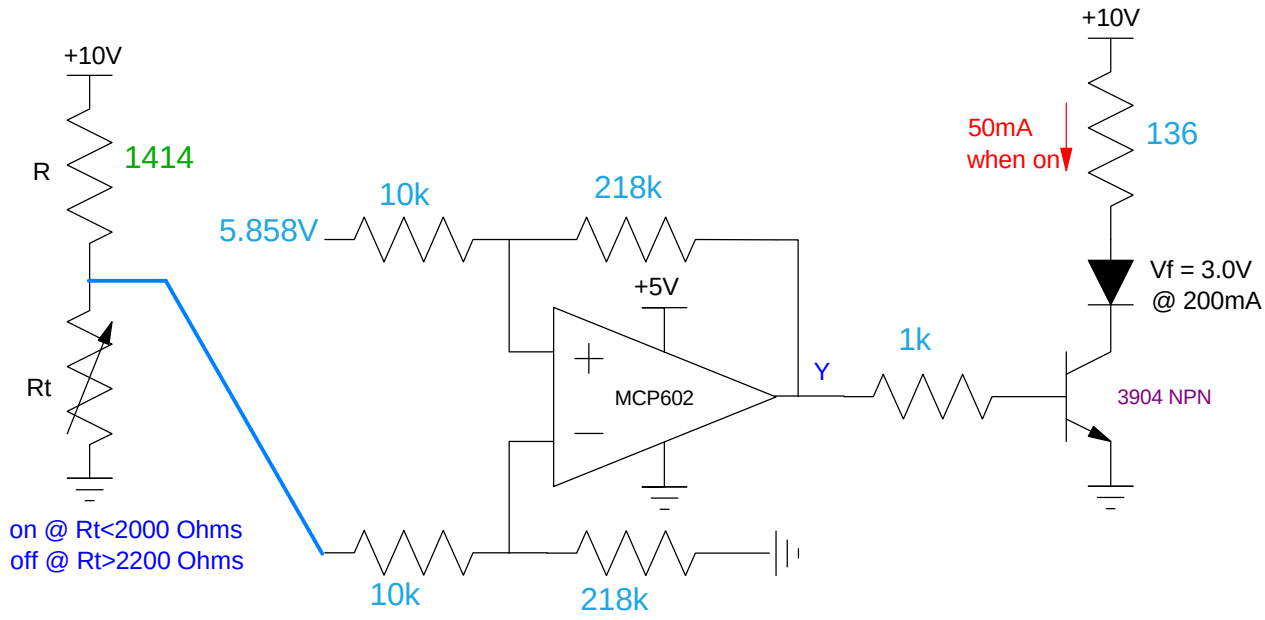


7) Design a Schmitt Trigger & transistor switch that

- Turns on the LED at 50mA when Rt < 2000 Ohms
- Turns off the LED when Rt > 2200 Ohms

Assume

- R = 900 + 100*(your birth month) + (your birth date)
- Vce(sat) = 0.2V
- Current gain (β) = 100



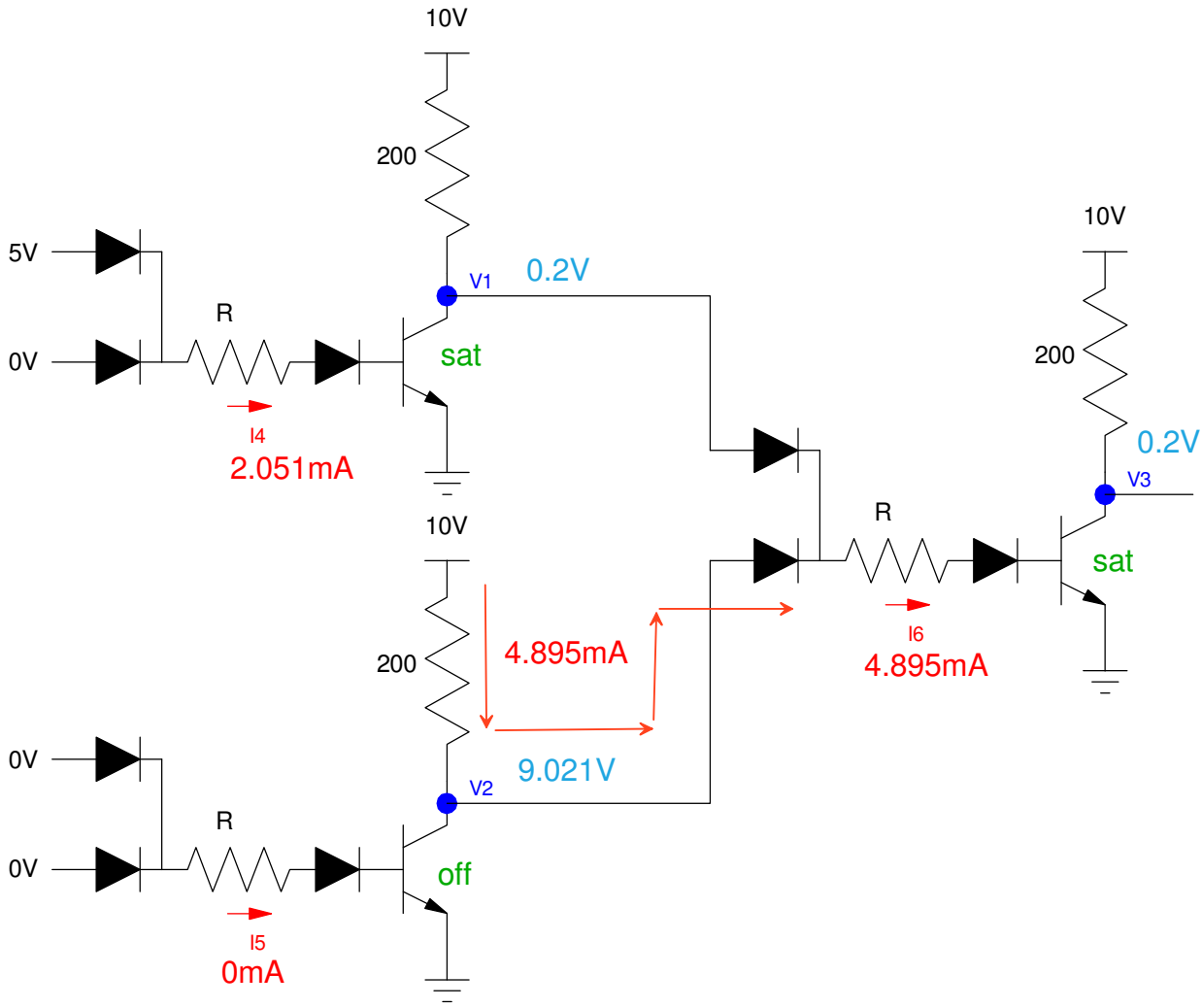
Rt = 2000:

-

8) DTL Logic: Determine the voltages and currents for the following DTL logic gage. Assume

- R = 900 + 100*(your birth month) + (birth day)
- Ideal silicon diodes (Vf = 0.7V), and
- Ideal 3904 transistors (Vbe = 0.7V, Vce(sat) = 0.2V, β=100)

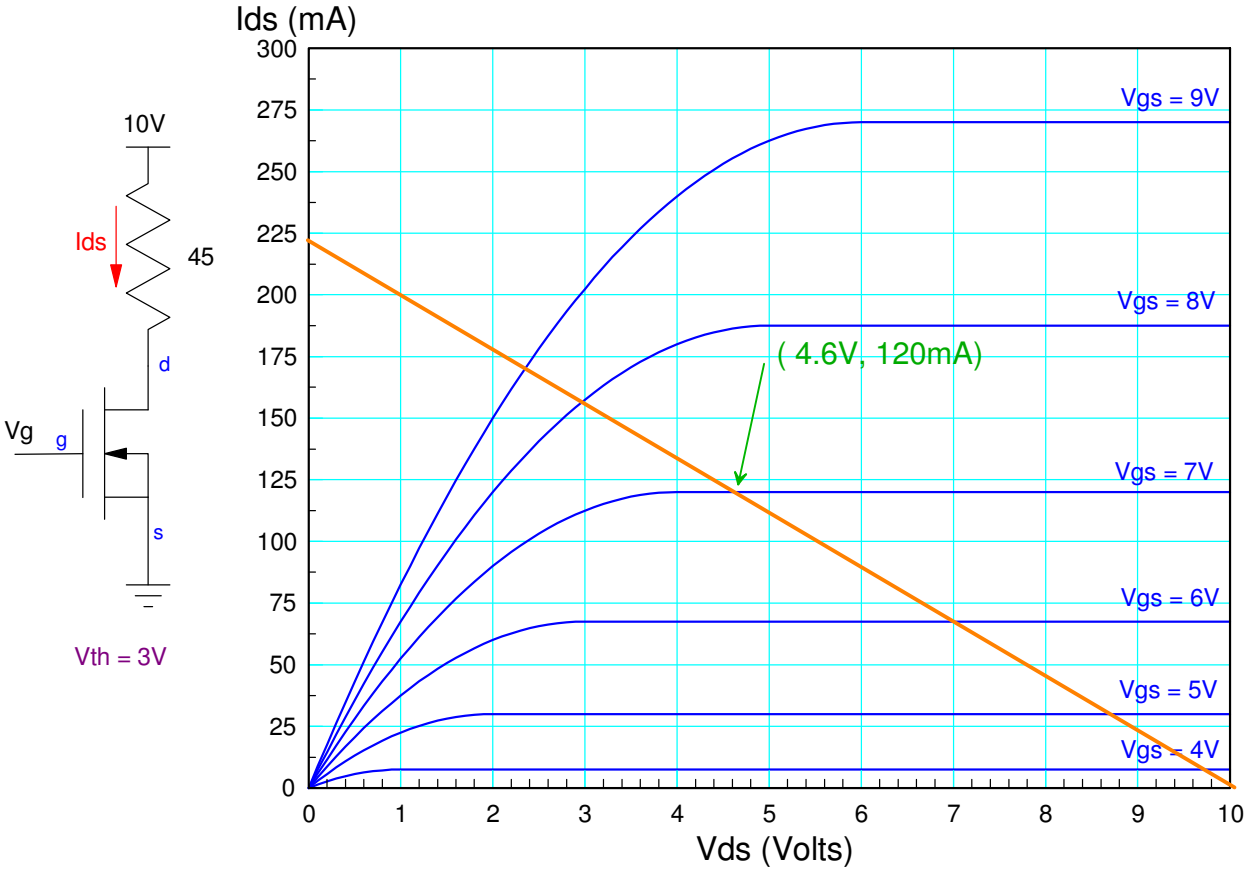
R 900 + 100*mo + da	V1	V2	V3	I4	I5	I6
1414	**0.2V** saturated	**9.021V** off	**0.2V** saturated	**2.051mA**	**0** off	**4.895mA**



9) MOSFET Load Line: For the following MOSFET circuit

- Determine the transconductance gain, kn,
- Draw the load line (x and y intercept), and
- Determine {Vds, Ids} when Vg = 7V

kn transconductance gain	Load Line x=intercept	Load Line y intercept	Vds Vg = 7V	Ids Vg = 7V	Operating Region off / active / ohmic
0.015 A/V2	**10V**	**222.2 mA**	**4.6V**	**120mA**	**saturated**



$$270mA = \frac{k_n}{2}(9V - 3V)^2$$

$$k_n = 0.015\frac{A}{V^2}$$

10) CMOS Logic

a) Design a CMOS logic gate to implement Y=f(A,B,C,D)

AB \ CD	00	01	11	10
00	0	0	1	1
01	x	0	x	0
11	0	x	x	0
10	1	1	0	0

$$\overline{Y} = B + \overline{A}\,\overline{C} + AC$$