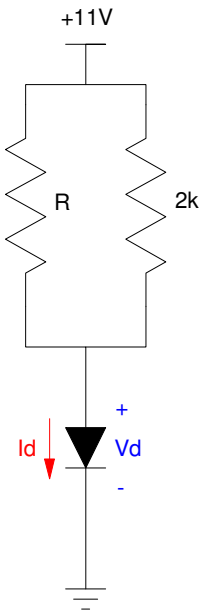
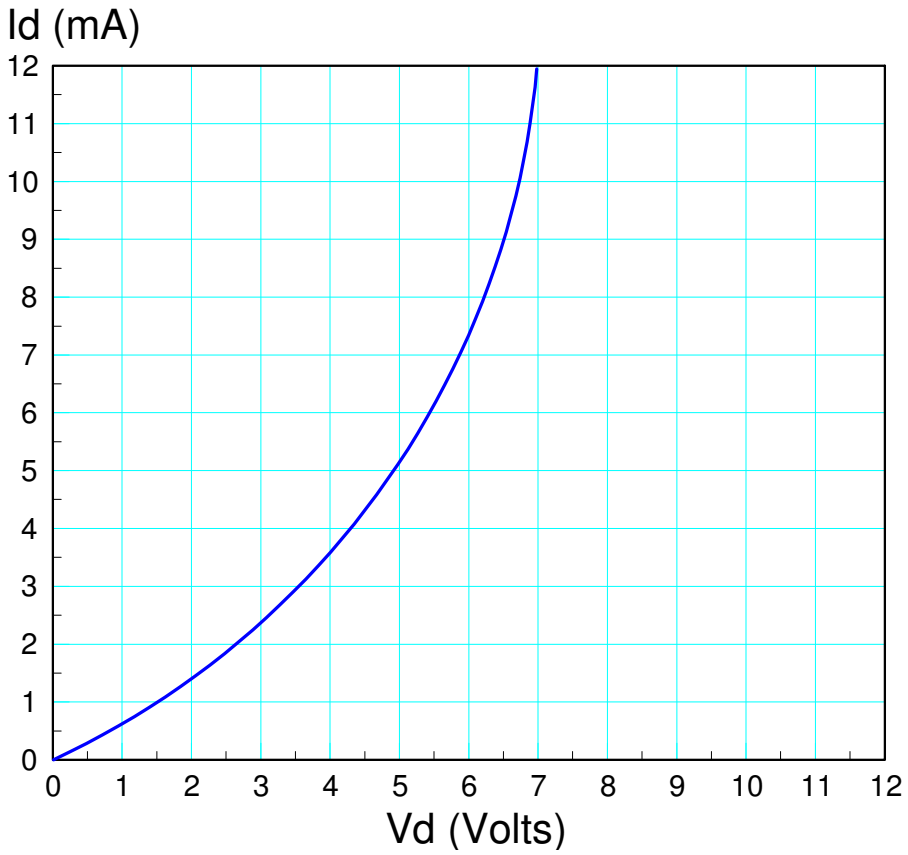
ECE 320 - Final (pt 1) - Name _____

Semiconductors & Diodes

1) Load Lines: Assume the VI characteristics for the diode is as shown in the graph. Draw the load line for the following circuit and determine Id and Vd. Assume R = 1000 + 100*(your birth month) + (your birth date).

R 1000 + 100*mo + day	Load Line x-intercept (volts)	Load Line y-intercept (mA)	Vd Volts	Id mA

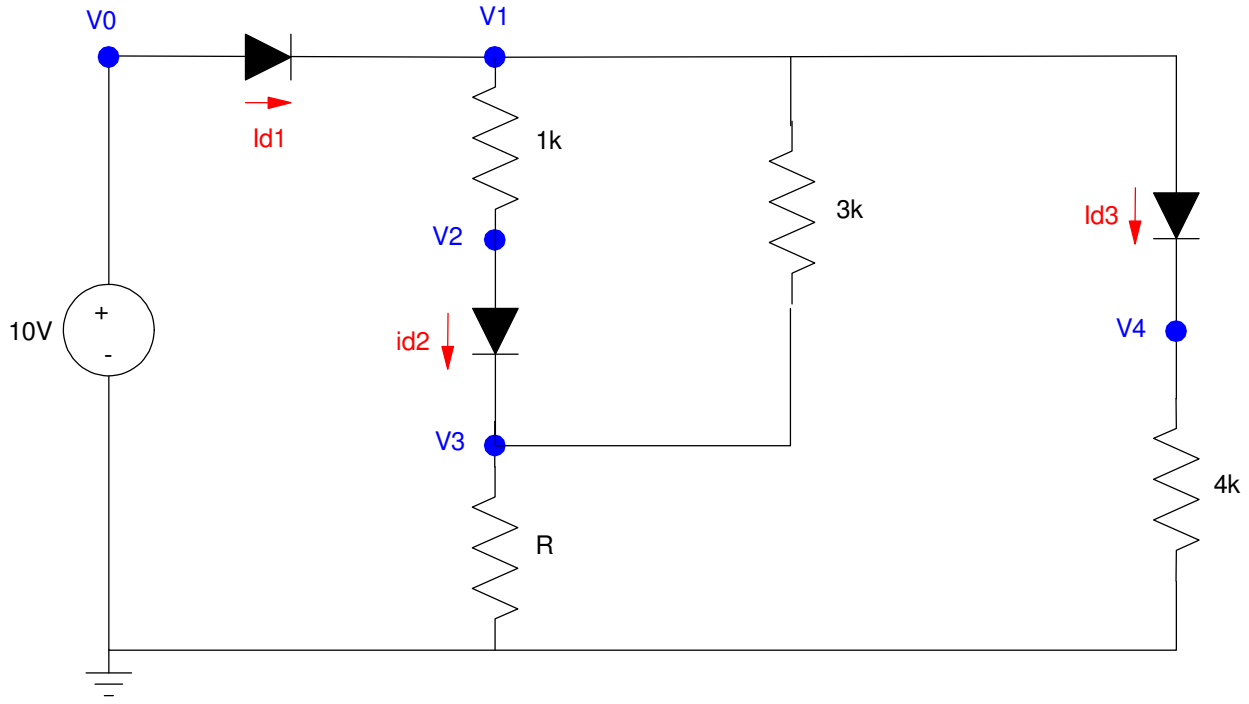




3) Ideal Silicon Diodes. Assume the diodes in this circuit are ideal silicon diodes:

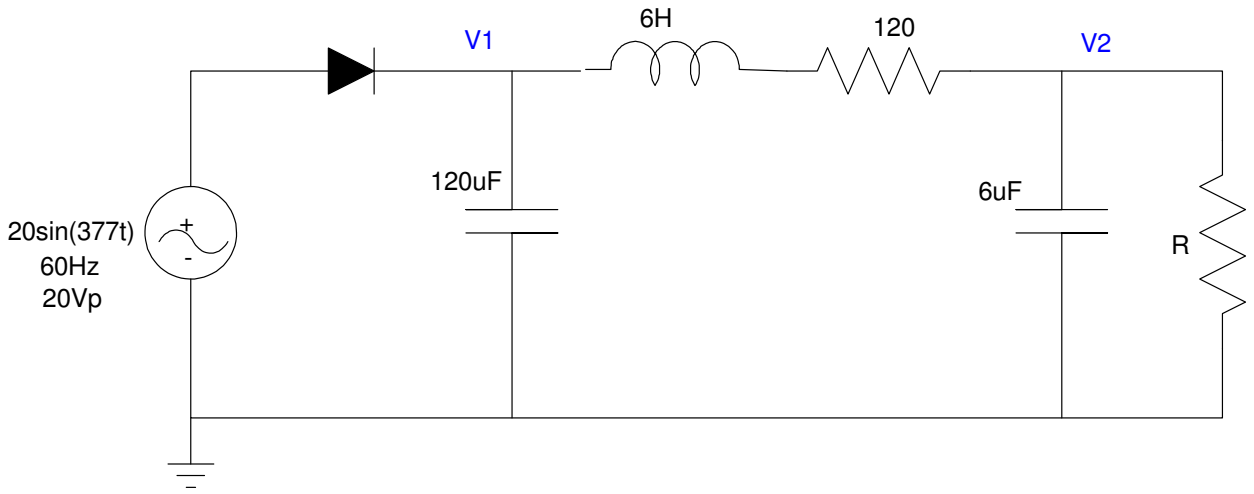
- Vd = 0.7V Id > 0
- Id = 0 Vd < 0.7V
- R = 1000 + 100*(your birth month) + (birth date). For example, May 14th gives 1514 Ohms.

R	Id1	V1	V2	V3	V4



4) AC to DC: Analysis: Determine V1 and V2 (both DC and AC) for the following AC to DC converter

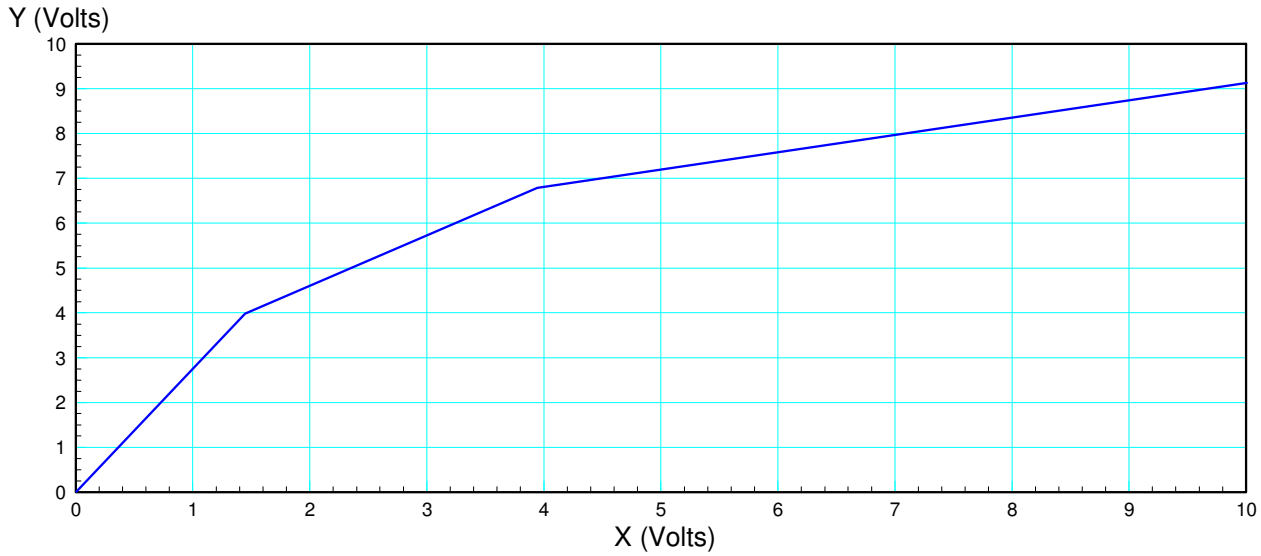
R	V1		V2	
	DC	AC	DC	AC

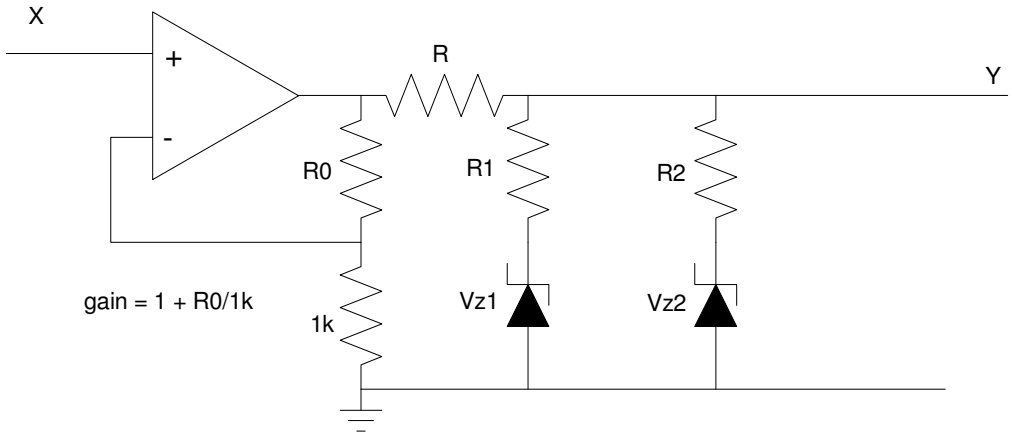


5) Clipper Circuit: Determine the resistors and zener votlages to implement the following function: Y = f(X). Assume

- Ideal silicon diodes (Vf = 0.7V)
- R = 1000 + 100*(your birth month) + (birth date)

R 1000 + 100*mo day	R0	R1	Vz1	R2	Vz2



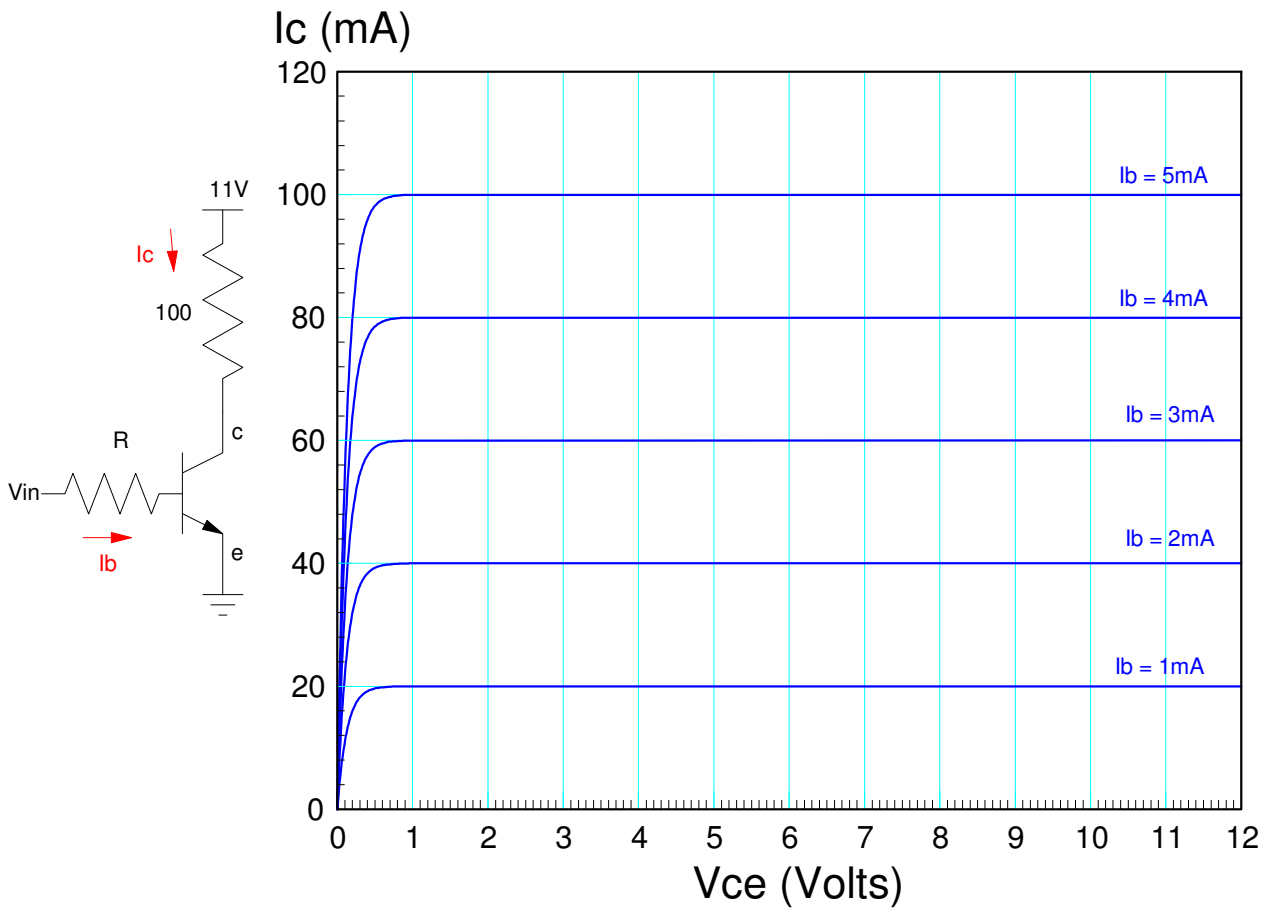


ECE 320 - Final (pt 2) - Name _____

Transistors and Mosfets

6) Determine the current gain, β. Also draw the load line and determine the operating point when Vin = 5V

R 1000 + 100*Mo + Day	Current Gain hfe = beta	Load Line x-intercept (Volts)	Load Line y-intercept (mA)	Vce Vin = 5V	Ic Vin = 5V

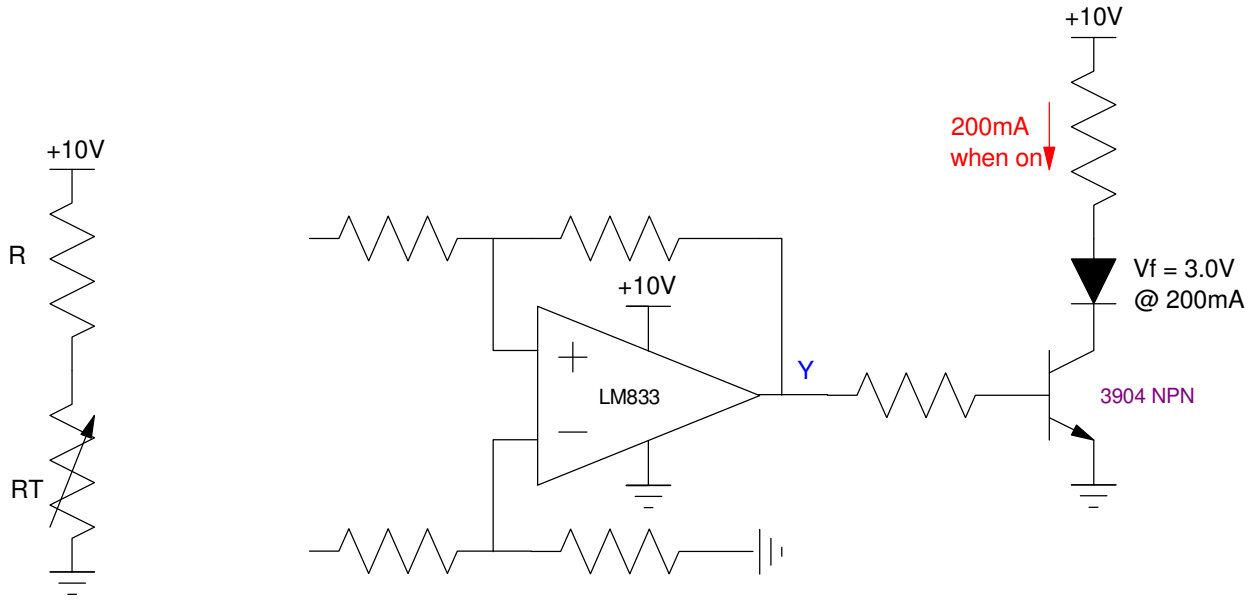


7) Design a Schmitt Trigger & transistor switch so that

- Turns on the LED at 200mA when RT > 1500 Ohms
- Turns off the LED when RT < 1200 Ohms

Assume

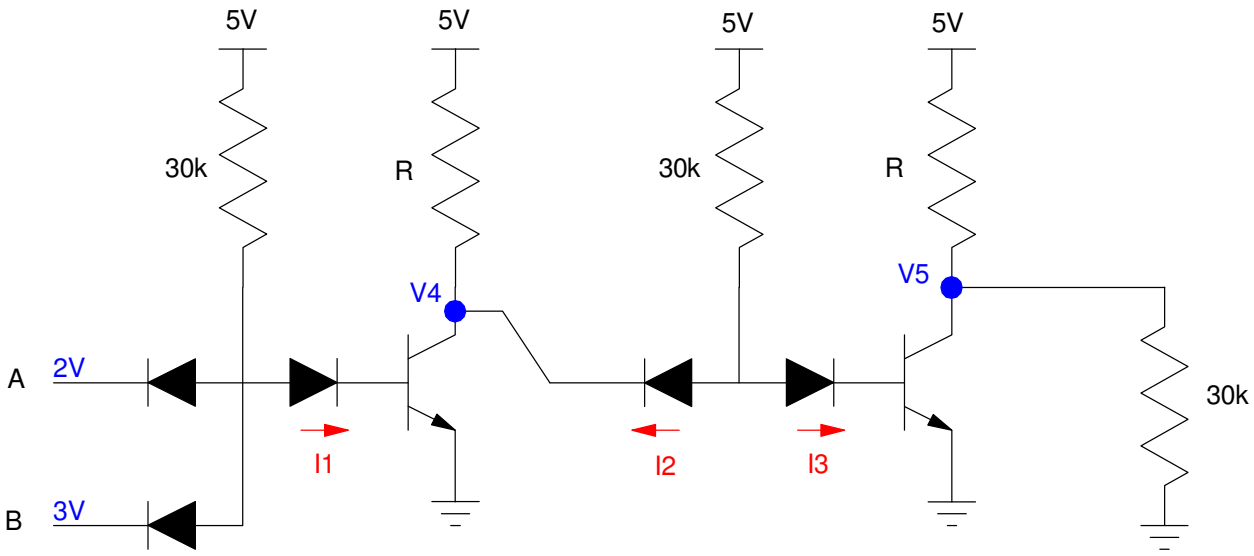
- R = 1000 + 100*(your birth month) + (your birth date)
- Vce(sat) = 0.2V
- Current gain (β) = 100



8) DTL Logic: Determine the voltages and currents for the following DTL logic gage. Assume

- R = 1000 + 100*(your birth month) + (birth day)
- Ideal silicon diodes (Vf = 0.7V), and
- Ideal 3904 transistors (Vbe = 0.7V, Vce(sat) = 0.2V, β=100)

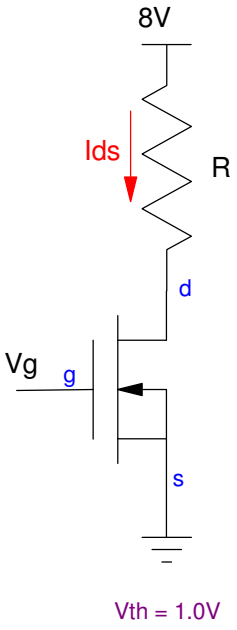
R 1000 + 100*mo + day	I1	I2	I3	V4	V5

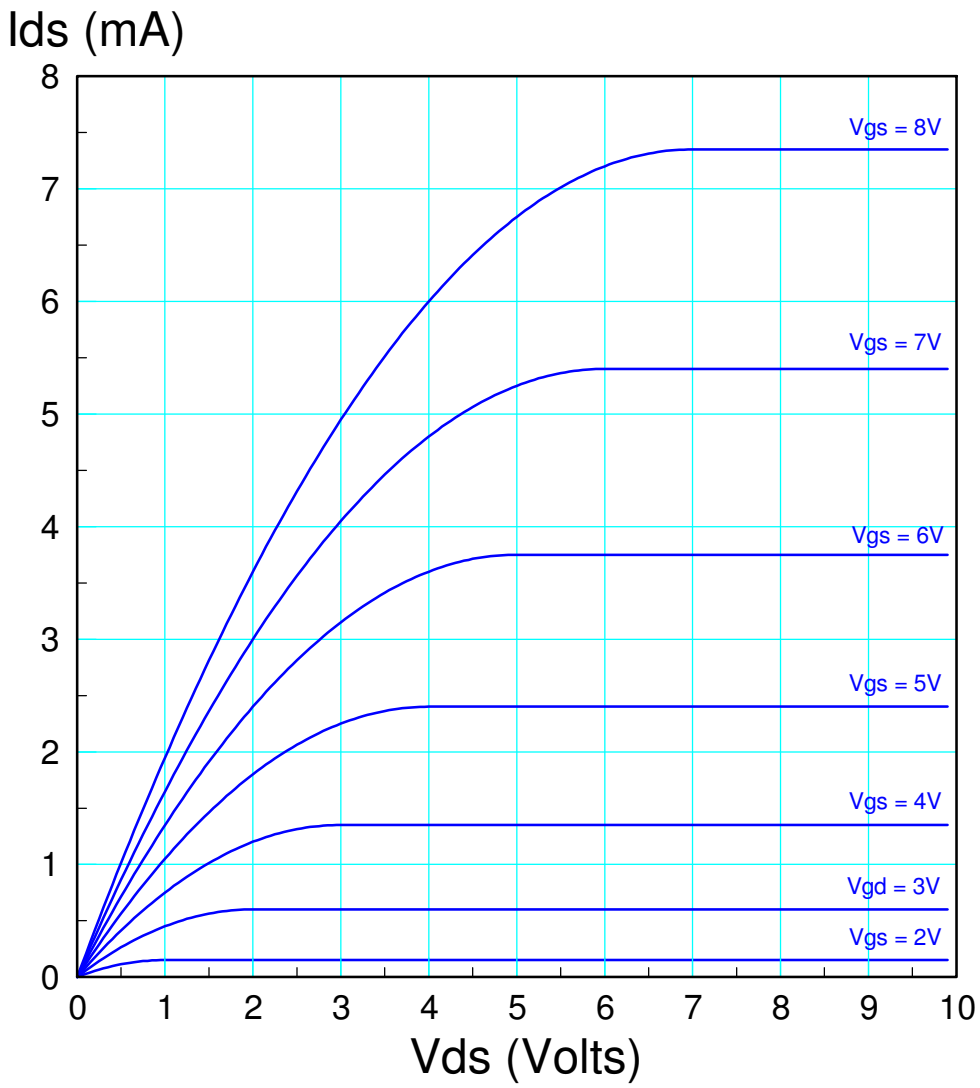


9) MOSFET Load Line: For the following MOSFET circuit

- Determine the transconductance gain, kn,
- Draw the load line (x and y intercept), and
- Determine {Vds, Ids} when Vg = 7V

R 1000 + 100*mo + day	kn transconductance gain	Load Line x=intercept	Load Line y intercept	Vds Vg = 7V	Ids Vg = 7V	Operating Region off / active / ohmic





10) CMOS Logic

a) Design a CMOS logic gate to implement Y=f(A,B,C,D)

AB \ CD	00	01	11	10
00	1	1	0	0
01	1	x	x	0
11	0	x	x	1
10	0	0	1	1