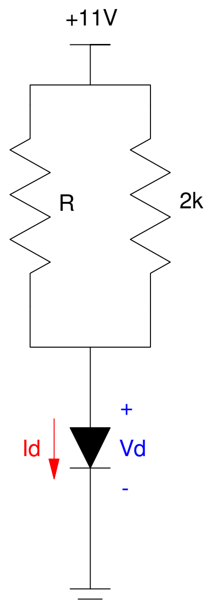
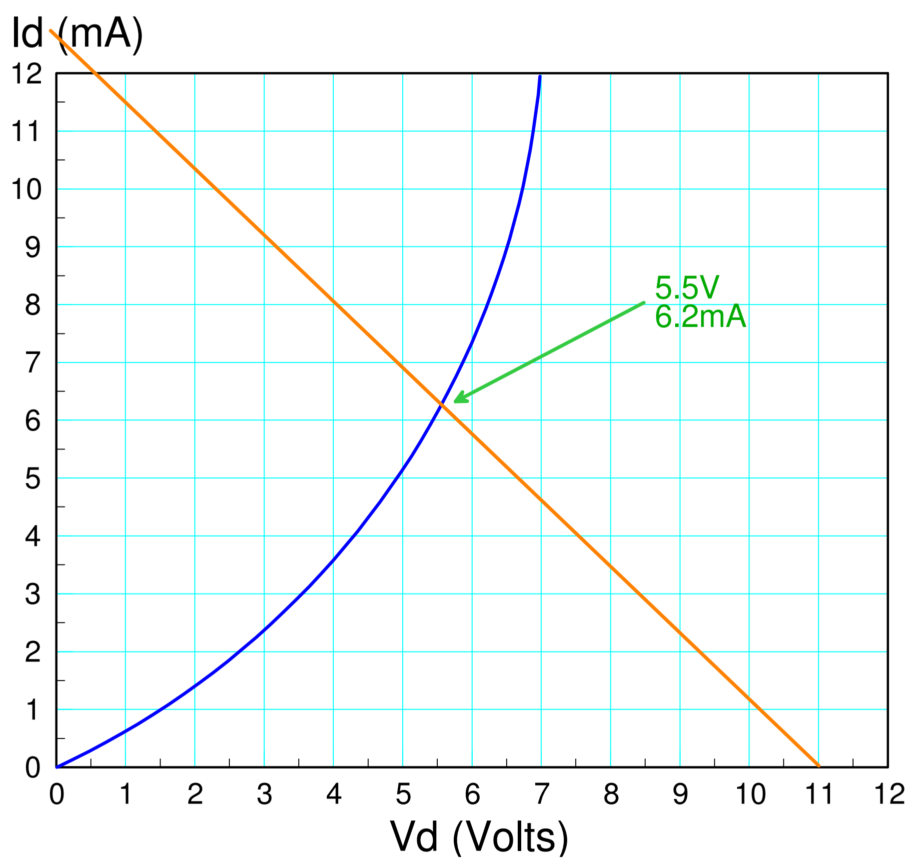
ECE 320 - Final (pt 1) - Name ____________________

Semiconductors & Diodes

1) Load Lines: Assume the VI characteristics for the diode is as shown in the graph. Draw the load line for the following circuit and determine Id and Vd. Assume R = 1000 + 100*(your birth month) + (your birth date).

R 1000 + 100*mo + day	Load Line x-intercept (volts)	Load Line y-intercept (mA)	Vd Volts	Id mA
1514	**11V**	**12.77mA**	**5.5V**	**6.2mA**





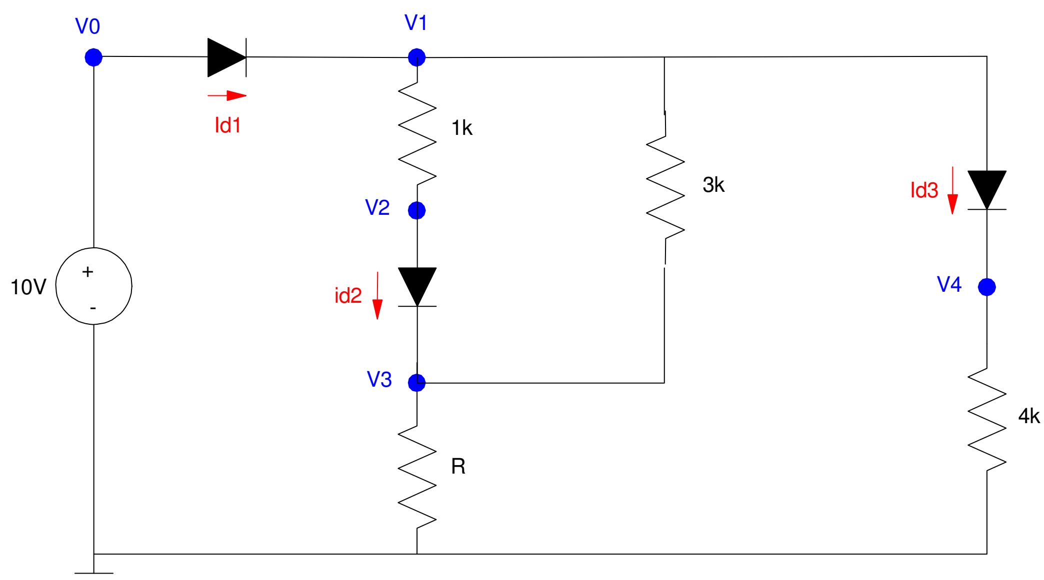
2) Nonlinear equations: Diode circuit

Assume the VI characteristics for the diodes shown below are

$$V_d = 0.052 \ln(10^8 \cdot I_d + 1) \qquad I_d = 10^{-8} \cdot \left(\exp\left(\frac{V_d}{0.052}\right) - 1\right)$$

Write N equations to solve for N unknonws: {V1, V2, V3, V4, Id1, Id2, Id3}.

- Note: you do not need to solve.
- R = 1000 + 100*(your birth month) + (birth date). For example, May 14th gives 1514 Ohms.



$$I_{d1} = 10^{-8} \cdot \left(\exp\left(\frac{V_0 - V_1}{0.052}\right) - 1\right)$$

$$I_{d2} = 10^{-8} \cdot \left(\exp\left(\frac{V_2 - V_3}{0.052}\right) - 1\right)$$

$$I_d = 10^{-8} \cdot \left(\exp\left(\frac{V_1 - V_4}{0.052}\right) - 1\right)$$

$$-I_{d1} + \left(\frac{V_1 - V_2}{1k}\right) + \left(\frac{V_1 - V_3}{3k}\right) + I_{d3} = 0$$

$$\left(\frac{V_2 - V_1}{1k}\right) + I_{d2} = 0$$

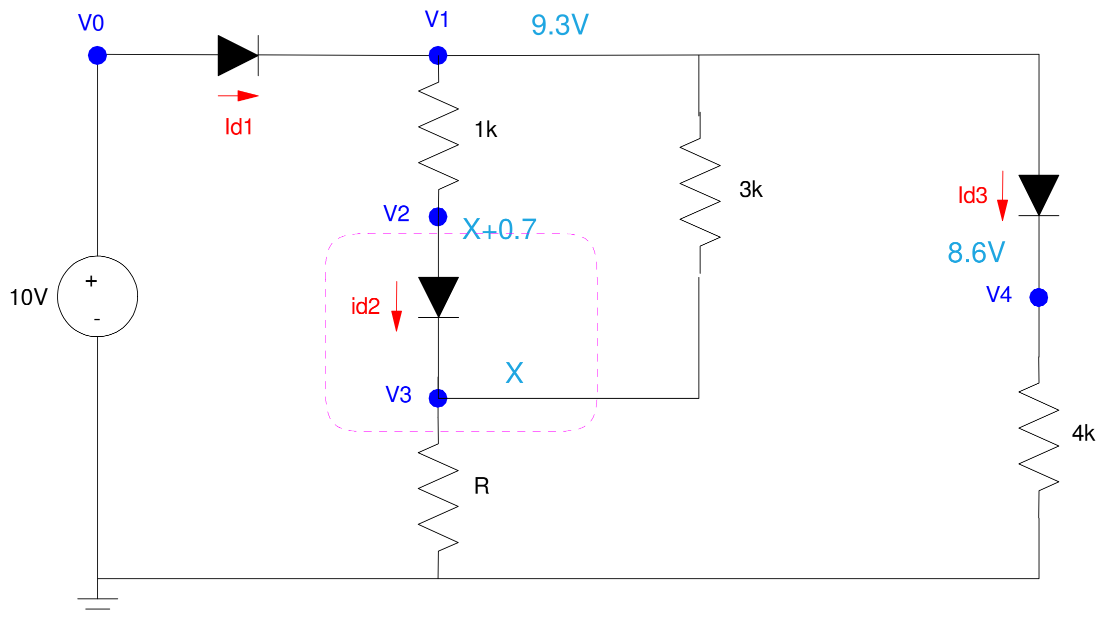
$$-I_{d2} + \left(\frac{V_3 - V_1}{3k}\right) + \left(\frac{V_3}{1514}\right) = 0$$

$$-I_{d3} + \left(\frac{V_4}{4k}\right) = 0$$

3) Ideal Silicon Diodes. Assume the diodes in this circuit are ideal silicon diodes:

- Vd = 0.7V   Id > 0
- Id = 0   Vd < 0.7V
- R = 1000 + 100*(your birth month) + (birth date). For example, May 14th gives 1514 Ohms.

R	Id1	V1	V2	V3	V4
1514	**6.026mA**	**9.3V**	**6.568V**	**5.868V**	**8.6V**



There is one unknown (V3). Writing the supernod equation

$$\left(\frac{V_3}{1514}\right) + \left(\frac{V_3 - 9.3}{3k}\right) + \left(\frac{(V_3 + 0.7) - 9.3}{1k}\right) = 0$$

$$V_3 = 5.868V$$

$$V_2 = V_3 + 0.7 = 6.568V$$

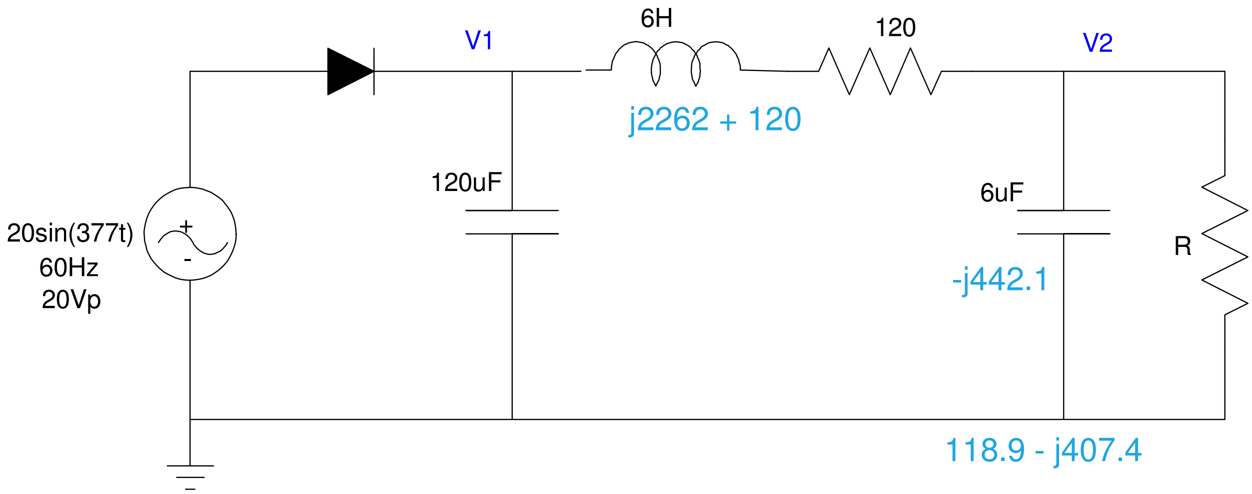
To find Id1

$$I_{d1} = \left(\frac{V_1 - V_2}{1k}\right) + \left(\frac{V_1 - V_3}{3k}\right) + \left(\frac{V_4}{4k}\right)$$

$$I_{d1} = 6.026mA$$

4) AC to DC: Analysis: Determine V1 and V2 (both DC and AC) for the following AC to DC converter

R	V1		V2	
	DC	AC	DC	AC
1514	**18.48V**	**1.640Vpp**	**17.12V**	**0.372Vpp**



max(V1) = 19.3V

$$I \approx \left(\frac{19.3V}{120+1514}\right) = 11.81mA \qquad \textit{worst case}$$

$$I = C\,\frac{dV}{dt}$$

$$11.81mA = 120\mu F \cdot \left(\frac{dV}{1/60s}\right)$$

$$dV = 1.640V_{pp} \qquad \textit{V1(AC)}$$

$$V_1(DC) = 19.3V - \tfrac{1}{2}\cdot 1.640V = 18.48V$$

$$V_2(DC) = \left(\frac{1514}{1514+120}\right) V_1(DC) = 17.12V$$

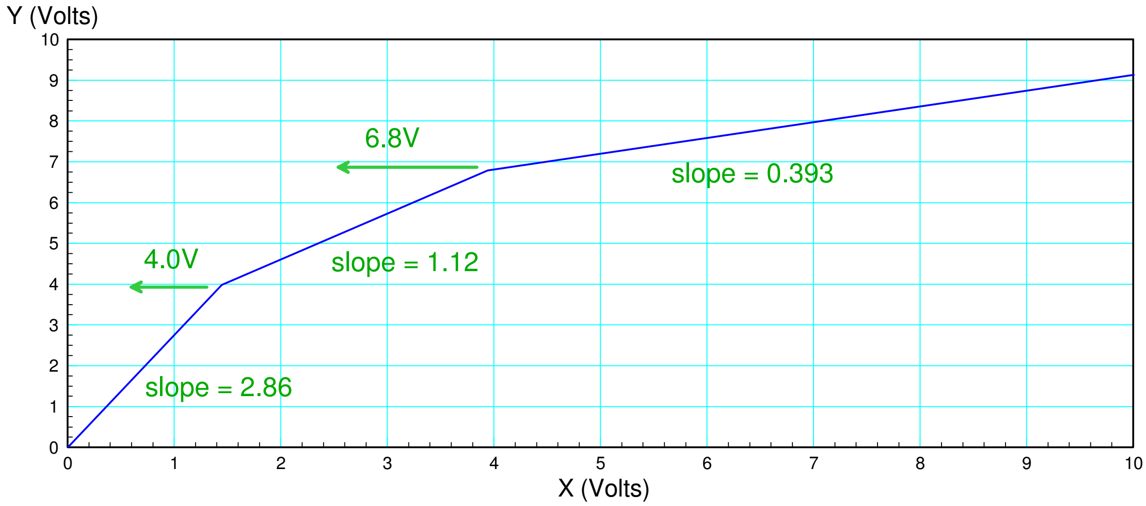
$$V_2(AC) = \left(\frac{(118.9-j407.4)}{(118.9-j407.4)+(120+j2262)}\right) V_1(AC)$$

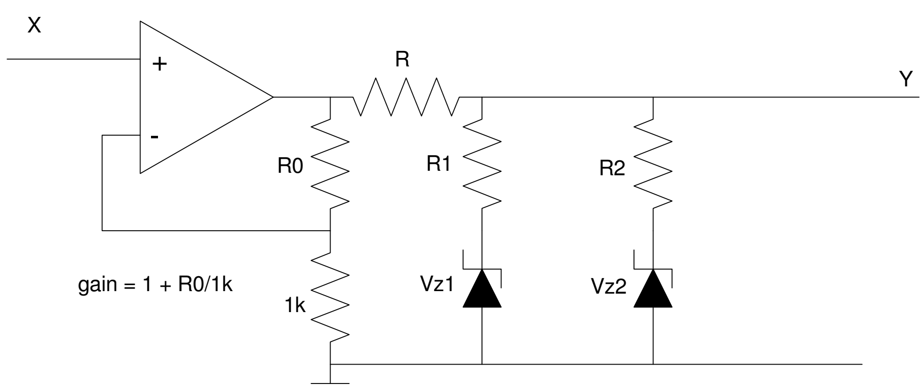
$$V_2(AC) = 0.372V_{pp}$$

5) Clipper Circuit: Determine the resistors and zener votlages to implement the following function: Y = f(X). Assume

- Ideal silicon diodes (Vf = 0.7V)
- R = 1000 + 100*(your birth month) + (birth date)

R 1000 + 100*mo day	R0	R1	Vz1	R2	Vz2
1514	**1.86k**	**974**	**4.0V**	**320**	**6.8V**





R1:

$$\left(\frac{R_1}{R_1+1514}\right)(2.86) = 1.12$$

$$R_1 = \left(\frac{1.12}{2.86-1.12}\right)1514 = 974\Omega$$

R2:

$$\left(\frac{R_{12}}{R_{12}+1514}\right)(2.86) = 0.393$$

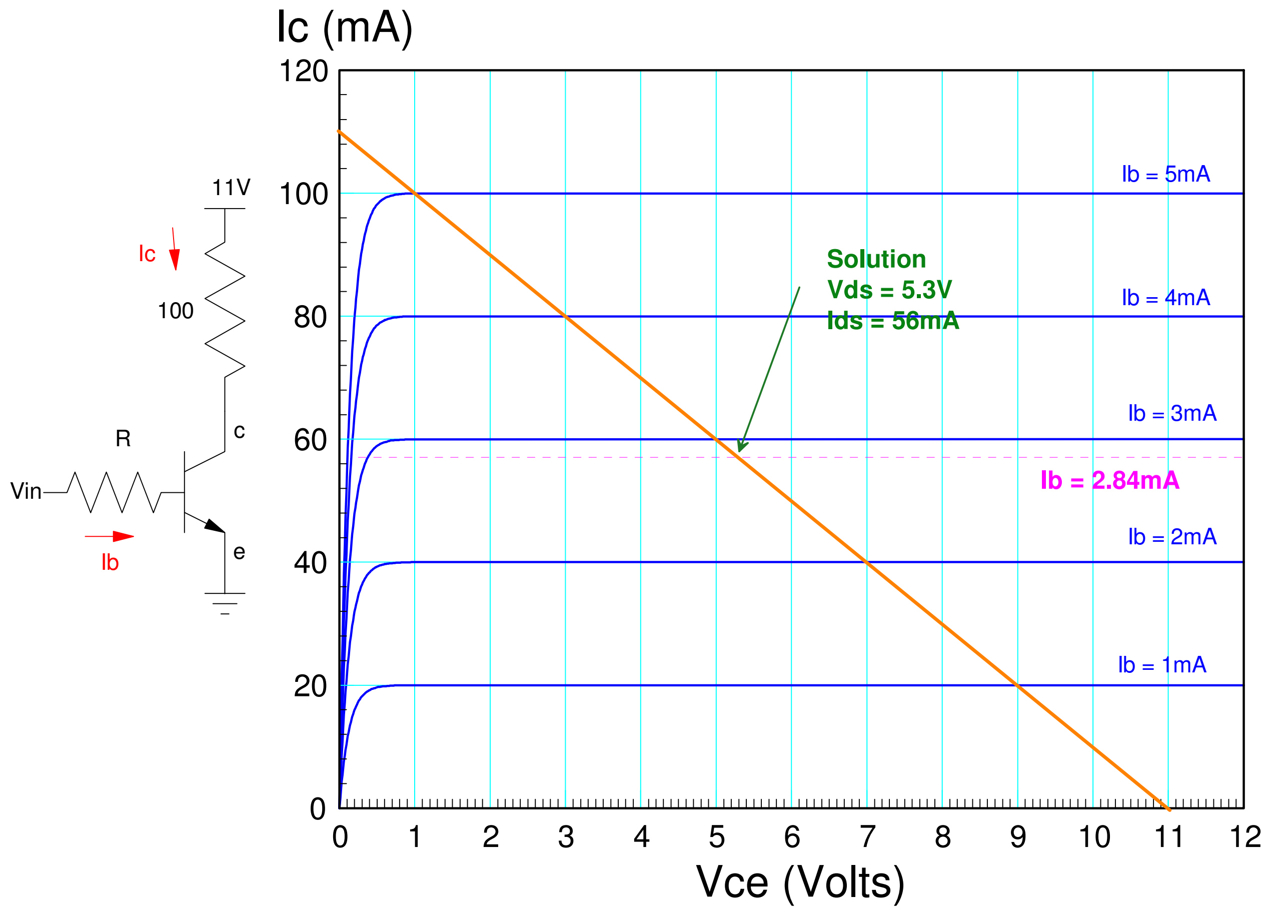
$$R_{12} = \left(\frac{0.393}{2.86-0.393}\right)1514 = 241.2\Omega$$

$$R_2 = 320.5\Omega$$

6) Determine the current gain, β. Also draw the load line and determine the operating point when Vin = 5V

R 1000 + 100*Mo + Day	Current Gain hfe = beta	Load Line x-intercept (Volts)	Load Line y-intercept (mA)	Vce Vin = 5V	Ic Vin = 5V
1514	**20**	**11V**	**110mA**	**5.3V**	**56mA**

$$I_b = \left(\frac{5V - 0.7V}{1514\Omega}\right) = 2.84mA$$

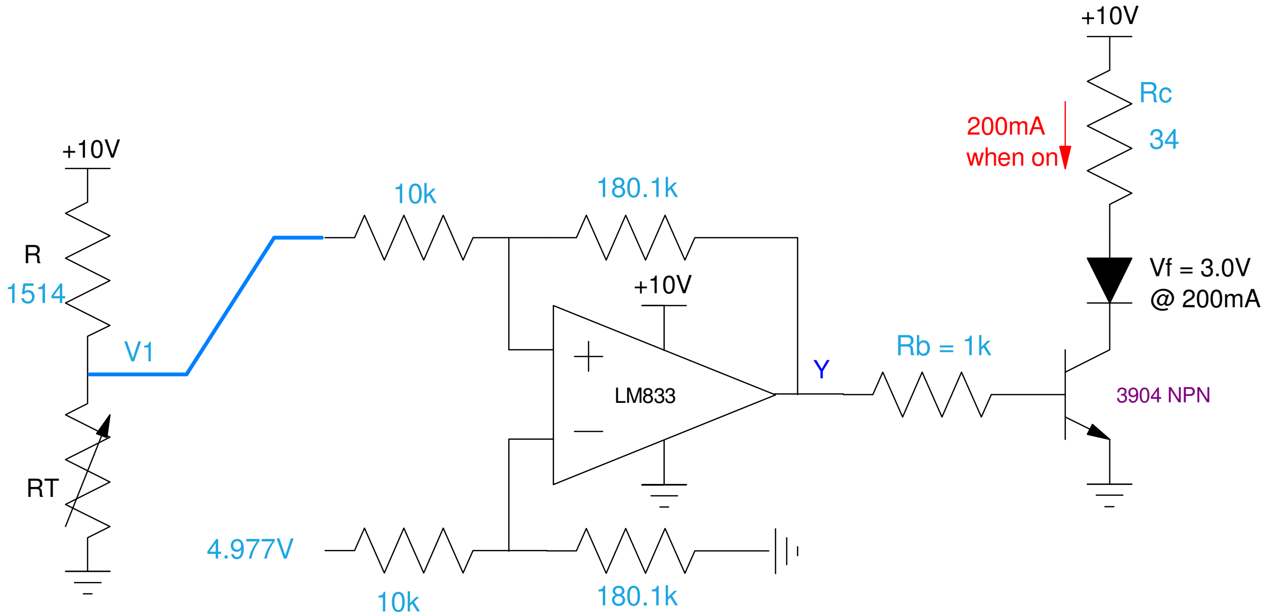


7) Design a Schmitt Trigger & transistor switch so that

- Turns on the LED at 200mA when RT > 1500 Ohms
- Turns off the LED when RT < 1200 Ohms

Assume

- R = 1000 + 100*(your birth month) + (your birth date)
- Vce(sat) = 0.2V
- Current gain (β) = 100



RT = 1500 Ohms

- $V_1 = \left(\frac{1500}{1500+1514}\right)10V = 4.977V$
- Y = 10

RT = 1200 Ohms

- $V_1 = \left(\frac{1200}{1200+1514}\right)10V = 4.422V$
- Y = 0V

$I_b > \frac{200mA}{\beta} = 2mA$

Let Ib = 9.3mA

$R_b = \left(\frac{10V-0.7V}{9.3mA}\right) = 1k$

$R_c = \left(\frac{10V-3V-0.2V}{200mA}\right) = 34\Omega$

Y goes down as V1 goes down (positive correlation). Connect to the + input.

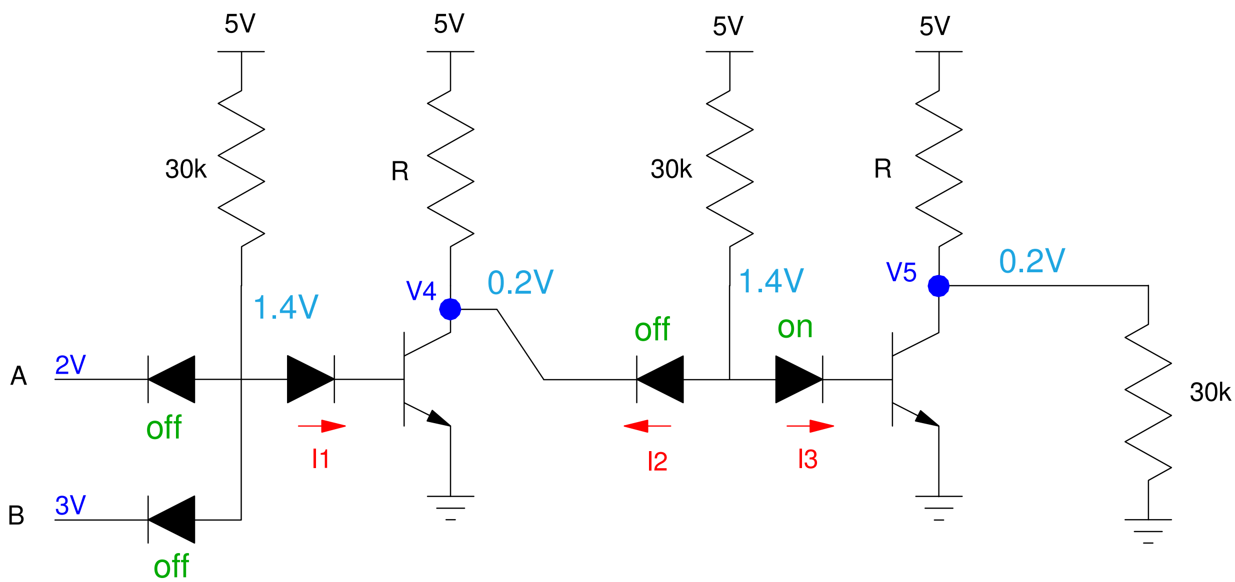
Gain is

$$gain = \left(\frac{10V-0V}{4.977V-4.422V}\right) = 18.01$$

8) DTL Logic: Determine the voltages and currents for the following DTL logic gage. Assume

- R = 1000 + 100*(your birth month) + (birth day)
- Ideal silicon diodes (Vf = 0.7V), and
- Ideal 3904 transistors (Vbe = 0.7V, Vce(sat) = 0.2V, β=100)

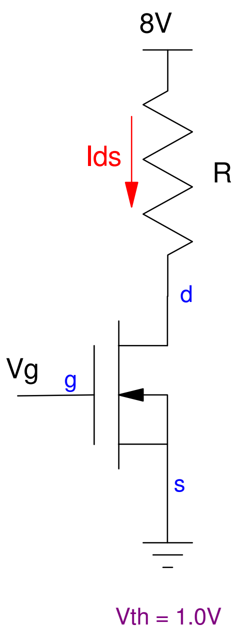
R 1000 + 100*mo + day	I1	I2	I3	V4	V5
1514	**2.38 mA**	**0**	**2.38mA**	**0.2V**	**0.2V**

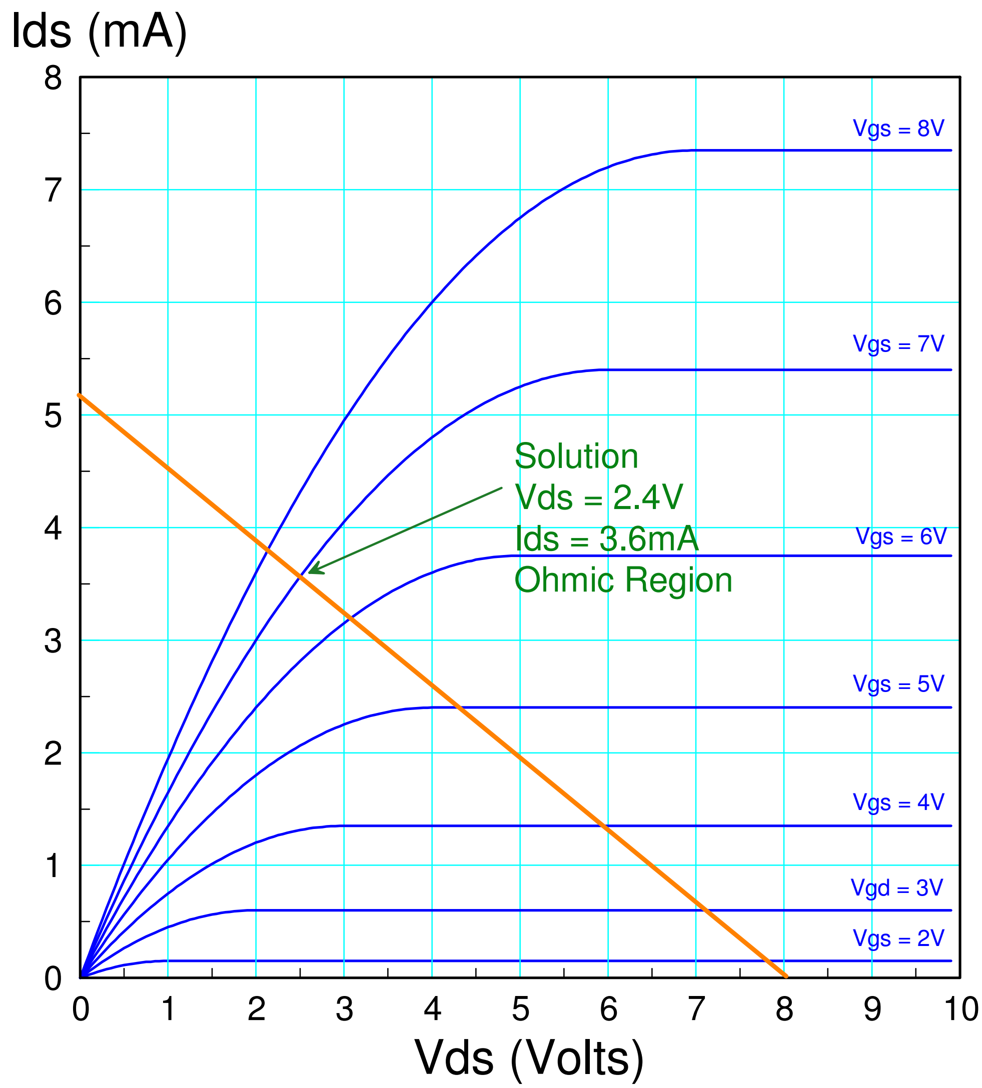


9) MOSFET Load Line: For the following MOSFET circuit

- Determine the transconductance gain, kn,
- Draw the load line (x and y intercept), and
- Determine {Vds, Ids} when Vg = 7V

R 1000 + 100*mo + day	kn transconductance gain	Load Line x=intercept	Load Line y intercept	Vds Vg = 7V	Ids Vg = 7V	Operating Region off / active / ohmic
1514	**298 uA/V²**	**8V**	**5.28mA**	**2.4V**	**3.6mA**	**ohmic**





kn calculations: Pick a point (Vs = 10V, Vgs = 8V, Ids = 7.3mA) . Region = saturated

$$I_{ds} = \frac{k_n}{2}(V_{gs} - V_{th})^2$$

$$7.3mA = \frac{k_n}{2}(8-1)^2$$

$$k_n = 298\frac{\mu A}{V^2}$$

10) CMOS Logic

a) Design a CMOS logic gate to implement Y=f(A,B,C,D)

AB \ CD	00	01	11	10
00	1	1	0	0
01	1	x	x	0
11	0	x	x	1
10	0	0	1	1

$$\overline{Y} = \overline{A}C + A\overline{C}$$

This is the logic on the low-side (n-channel MOSFETs)

from DeMorgan's law

$$Y = \left(A + \overline{C}\right)\left(\overline{A} + C\right)$$

This is the logic for the high-side (p-channel MOSFETs)